ATLAS,ALICE等大規模実験における信号処理高度化の実例

狩野博之

ASIC化の利点

大規模SYSTEMを如何に実現させるか

高速化 (ATLAS)

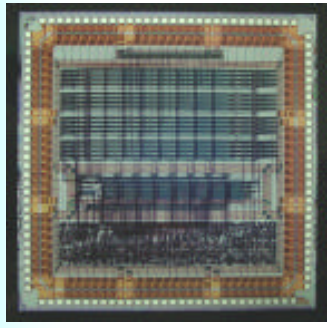
Systemの多Channel化 (ATLAS)

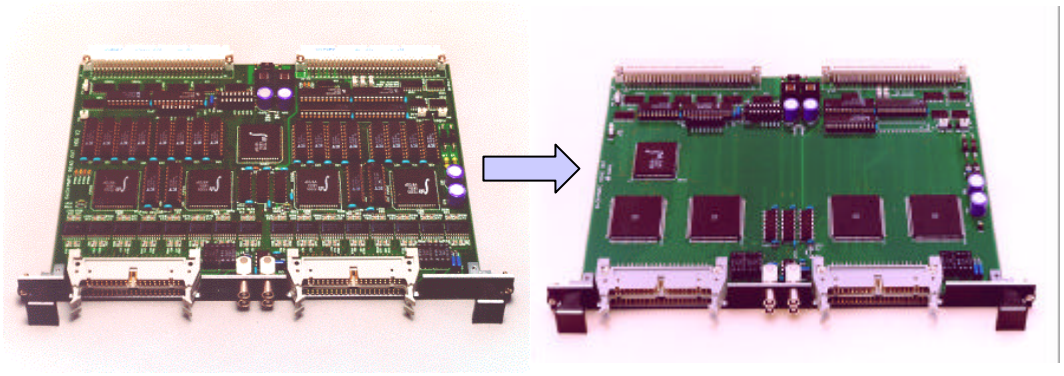
限られたスペースへ如何に効率よく設置するか

更なる省スペース化への努力 (ALICE)

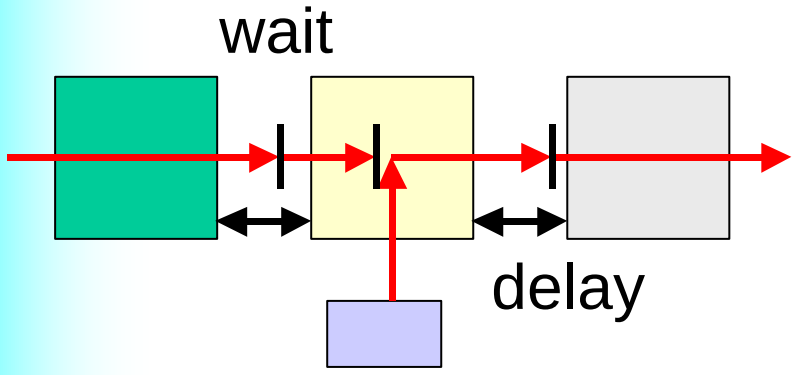
処理すべき信号の増加、処理速度の高速化

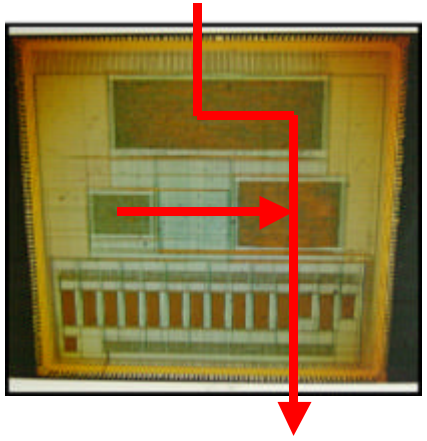
ASIC : Increasing channels per area

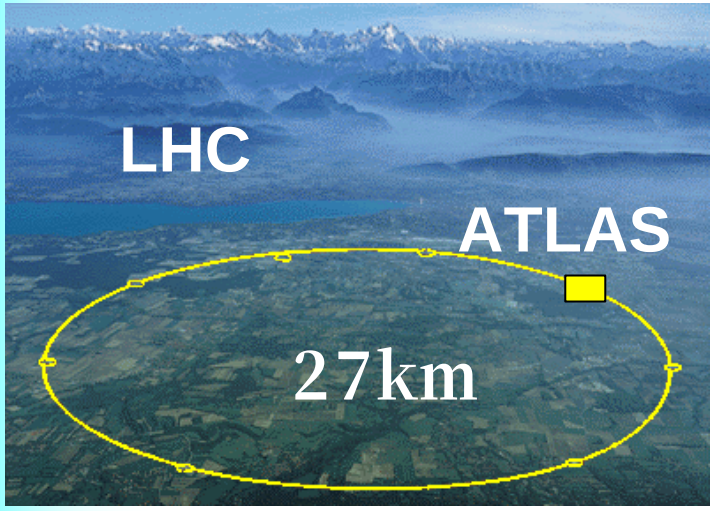


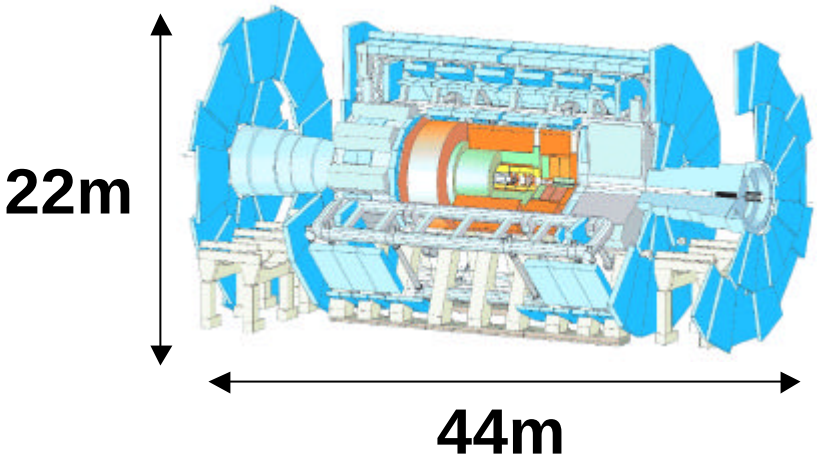


Integration : decreasing timing loss









Parameter Table

Name	Rate	Luminosity	# of ch	Speed
LEP	10～20ms	10^{31}	10^{4}	100
Tevatron	132ns	5×10^{30}	10^{5}	5×10^{4}
LHC	25ns	10^{34}	10^{7}	10^{6}
		$cm^{-2}s^{-1}$		MIPS

⇒ S/N=1/1,000,000

3-LEVEL Trigger System

3 LEVEL Trigger

LEVEL-1：

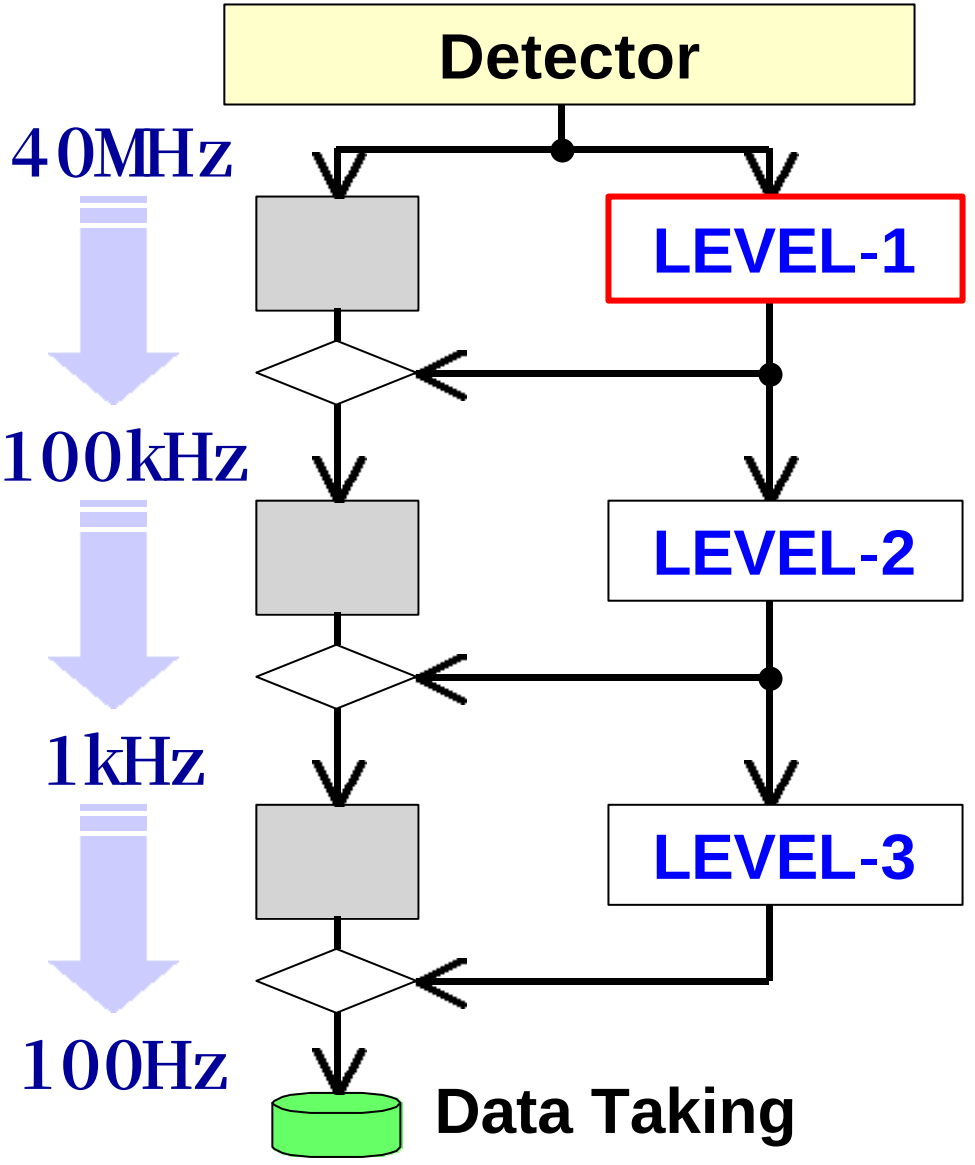
Hardware

LEVEL-2：

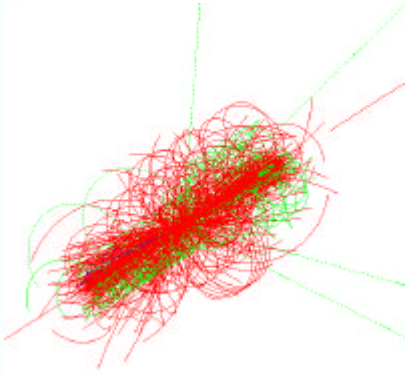
Hardware + software

LEVEL-3：

Software

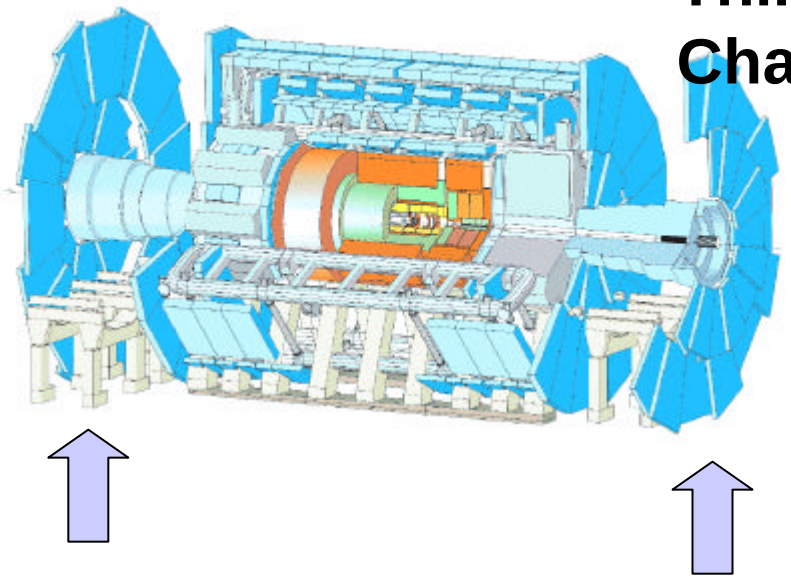


Interested event

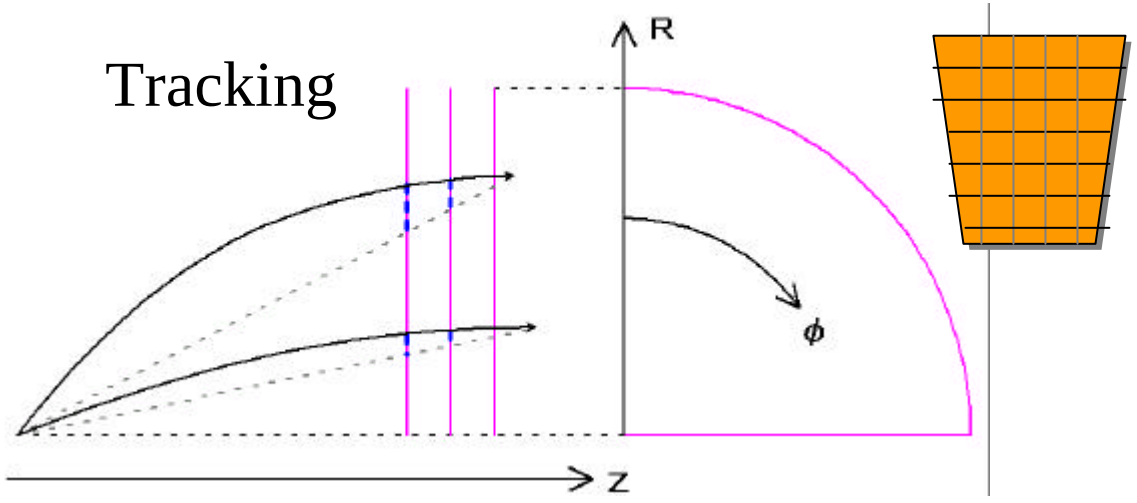


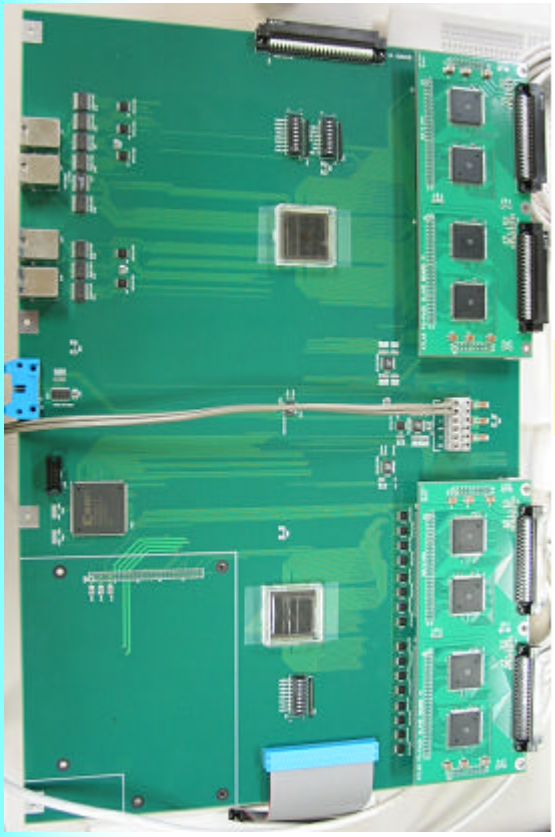
Trigger signal

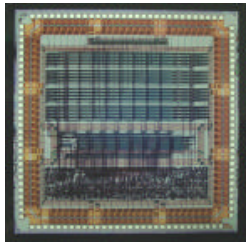
Thin Gap Chamber



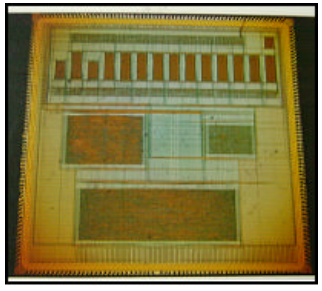
Tracking



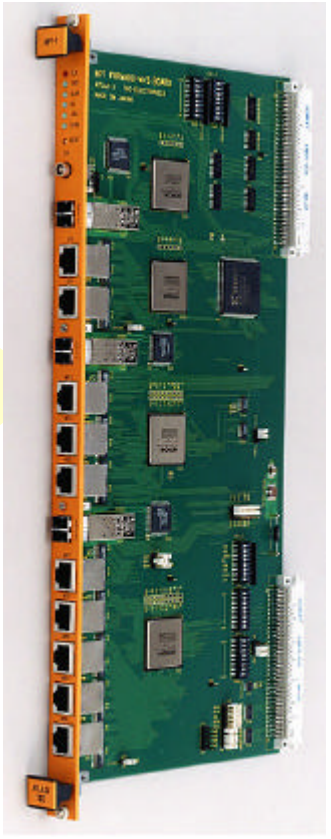


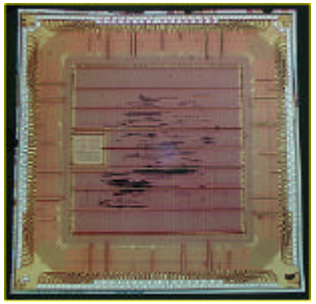


Timing Chip



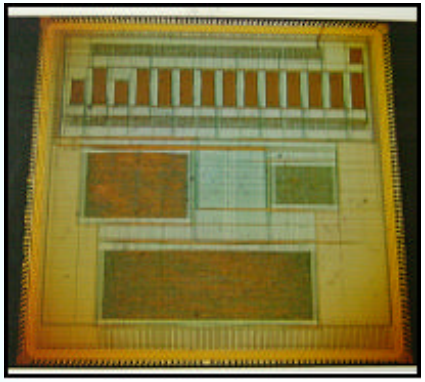
Readout Chip





Trigger Chip

This set covers 256 inputs.



Readout chip

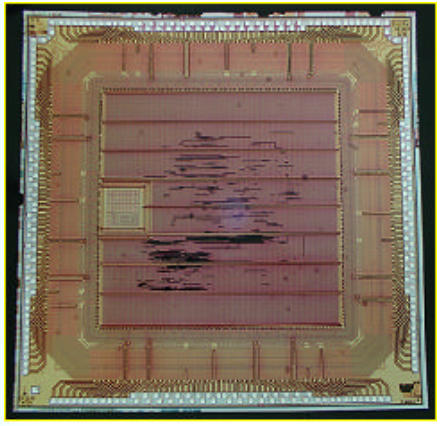
Multi block :

several functional blocks

-work sharing

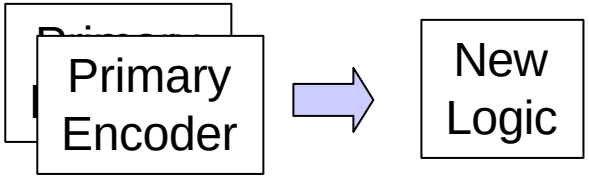
-Analog/Digital separation

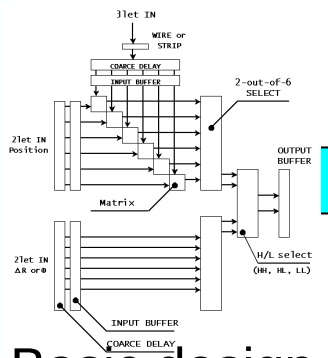
-common core



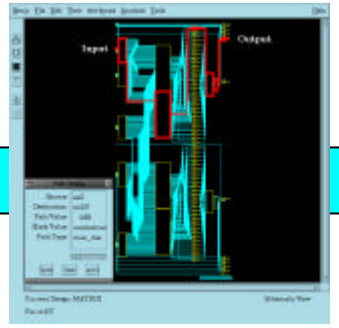
Trigger chip

Parallel Tasking



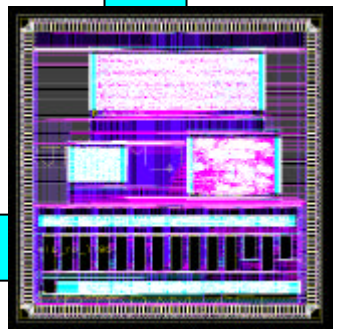


Basic design



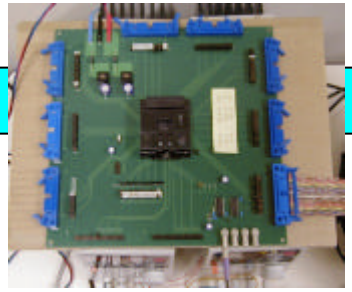
Logic design

Timing design

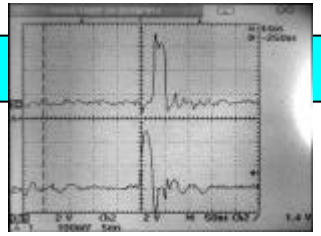


P&R Design

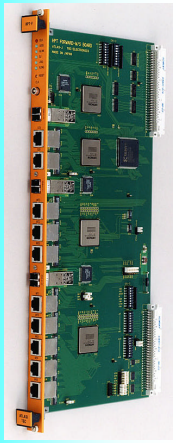
Production



Func. Test



Spec. Test



Complete

Cost of SLB ASIC (ATLAS)

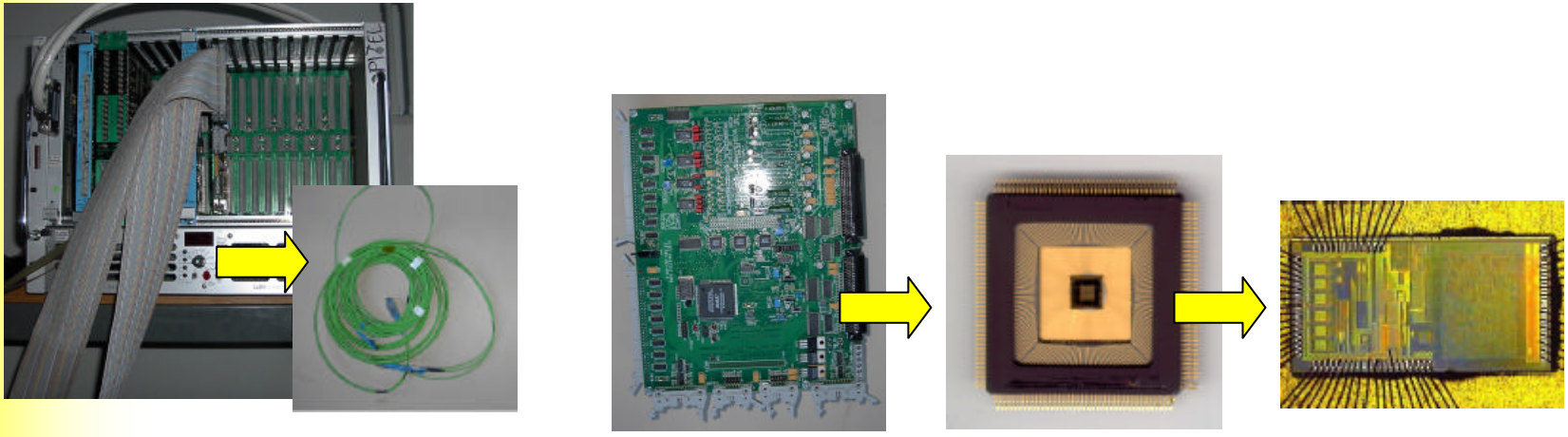
All except production block : ¥20,000,000

Basic design only : ¥100,000,000

限られた設置空間　→　如何に実現させるか？

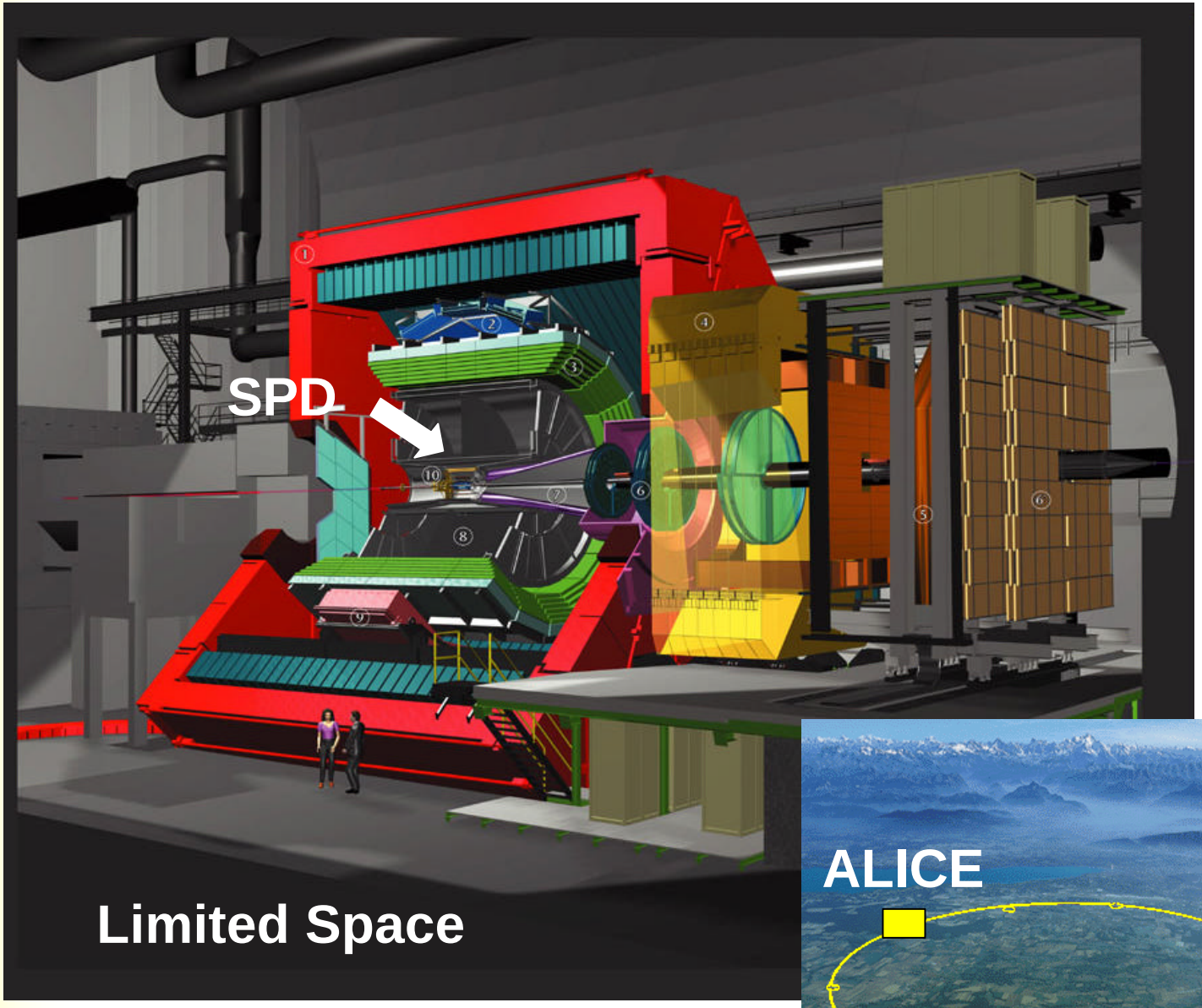
DATA Transmission : serialize data, optical cable

Front-end Electronics : Wire bonding, Custom IC

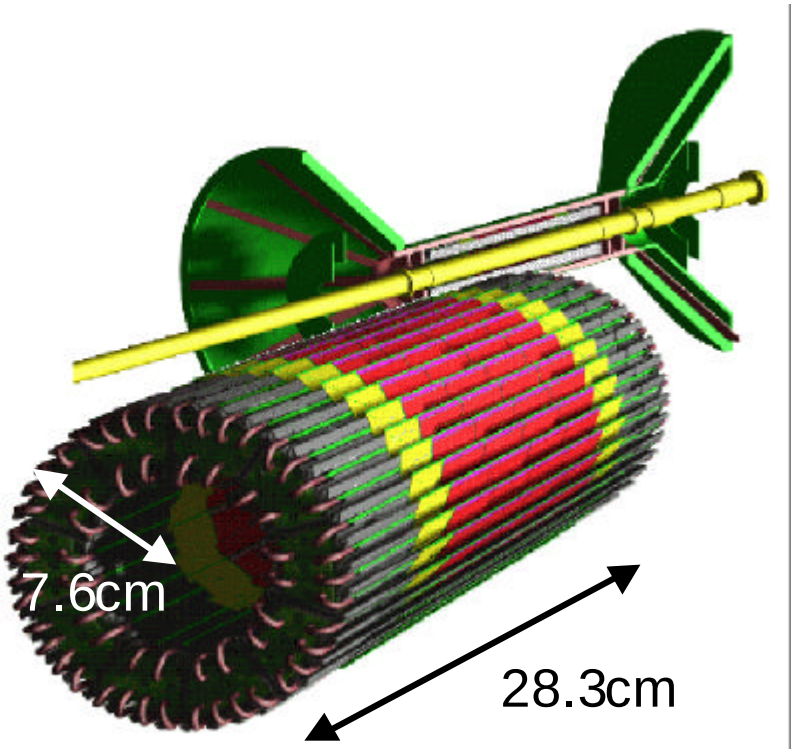


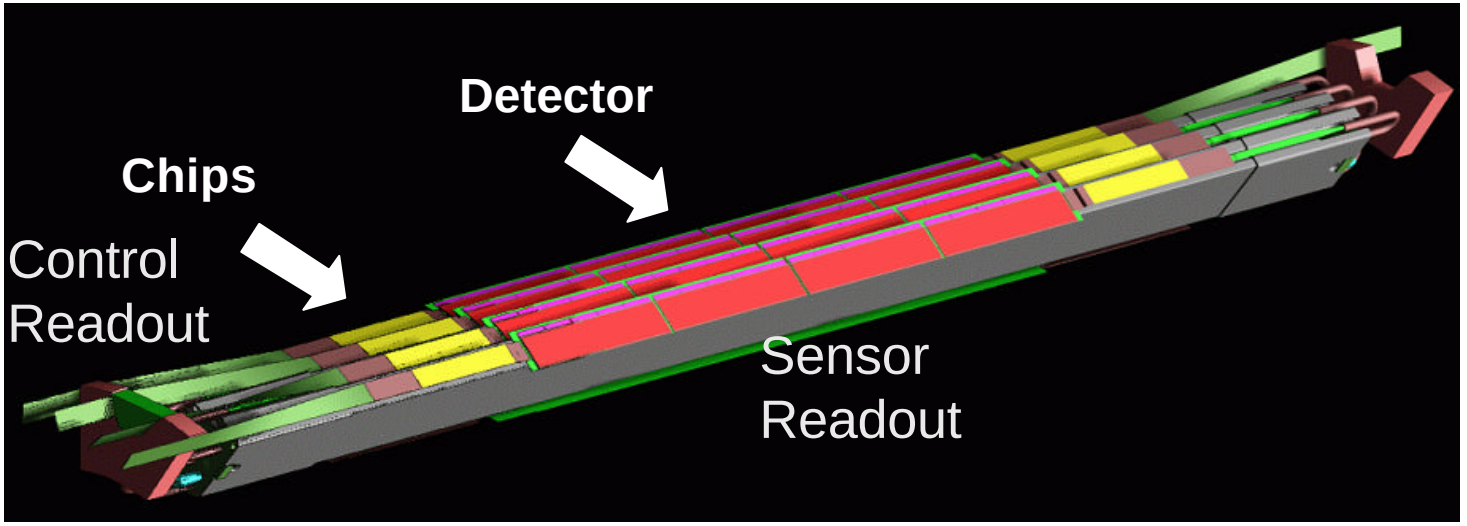
ALICE SPD

ALICE Experimental Setup



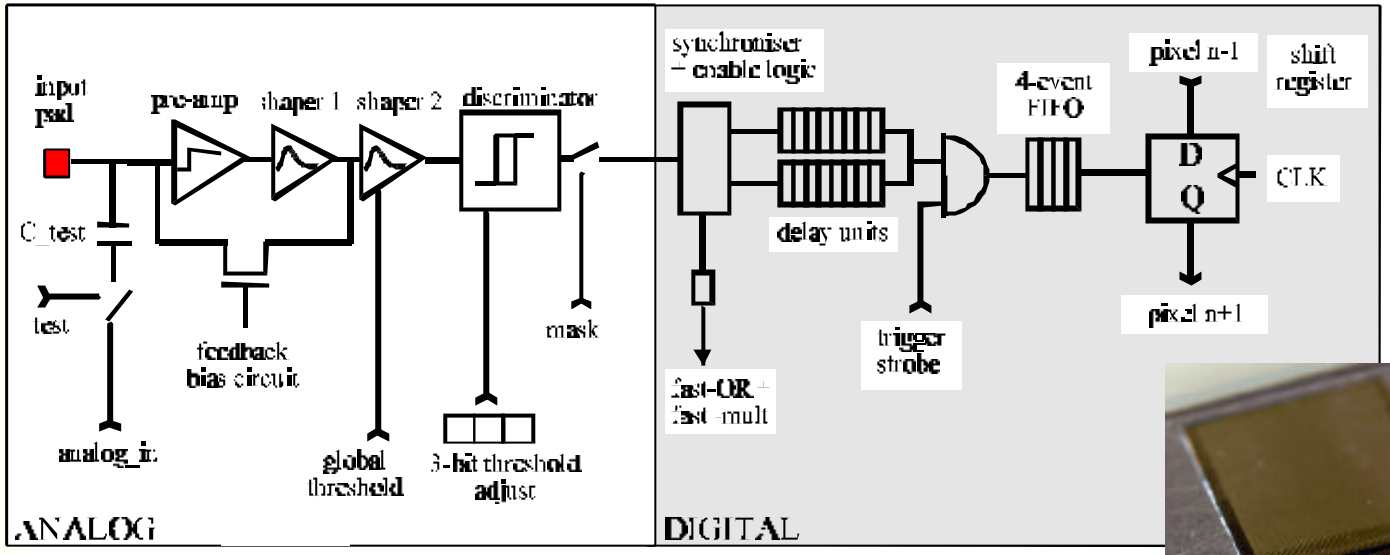
ALICE PIXEL Detector





ALICE ASICs

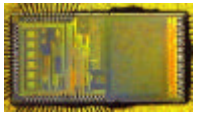
Pixel Cell



32x256 Cells

Analog Pilot Chip

Power control, Environmental monitor

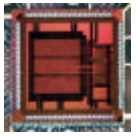


Digital Pilot Chip

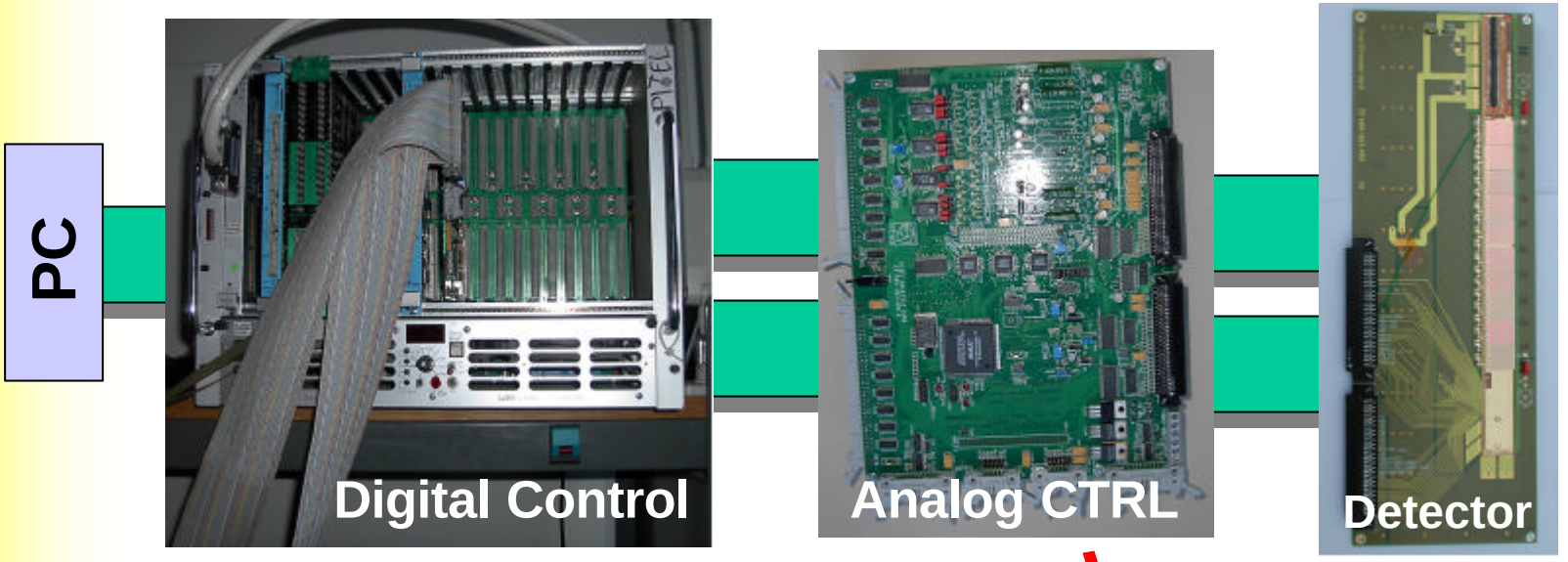
Chip Control, Data Control

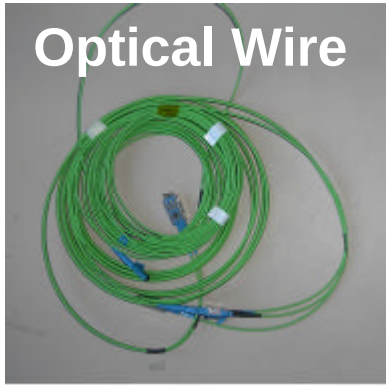
Serializer Chip

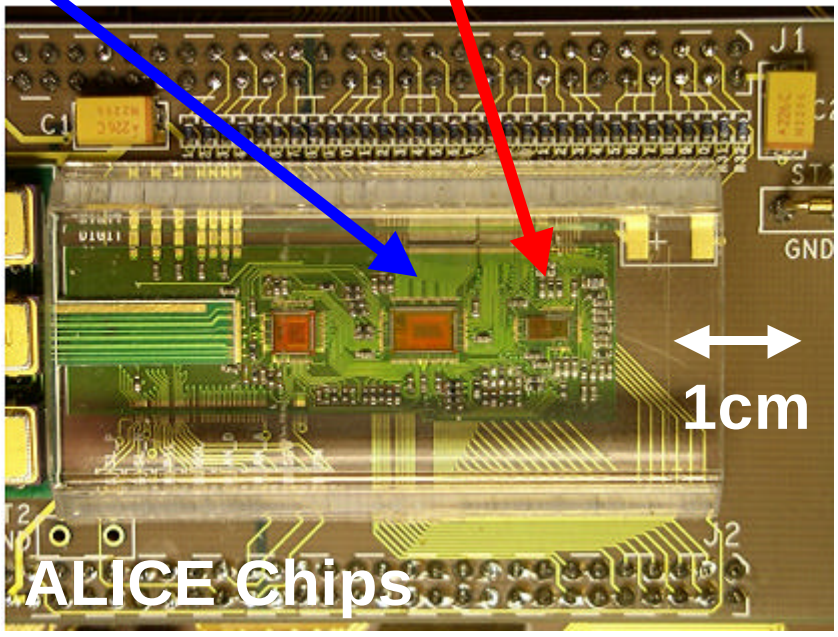
Serializer for optical link



ALICE Readout & Control System

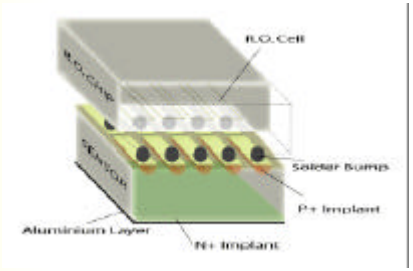


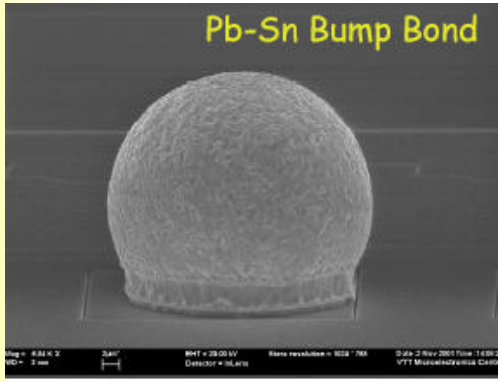




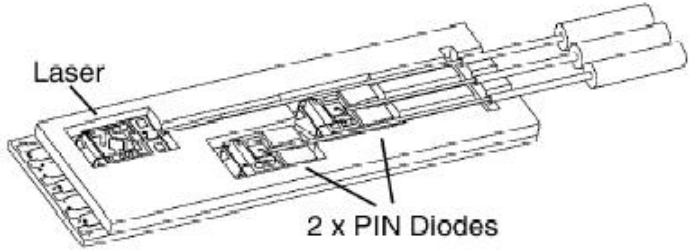
More Effort

Bump Bonding

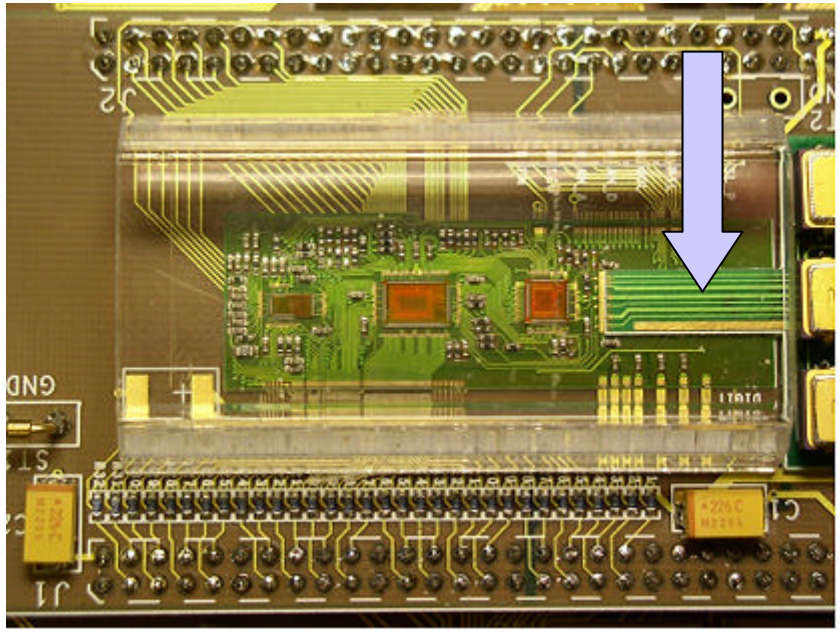




Custom Optical Component



16mm x 6mm x 1.2mm



SUMMARY

- コストと開発時間が必要ではあるものの検出器の飛躍的な高性能化にASICは必要不可欠である
- ATLAS, ALICE実験においてASICシステムはシビアな要求を十分満たす性能を発揮している