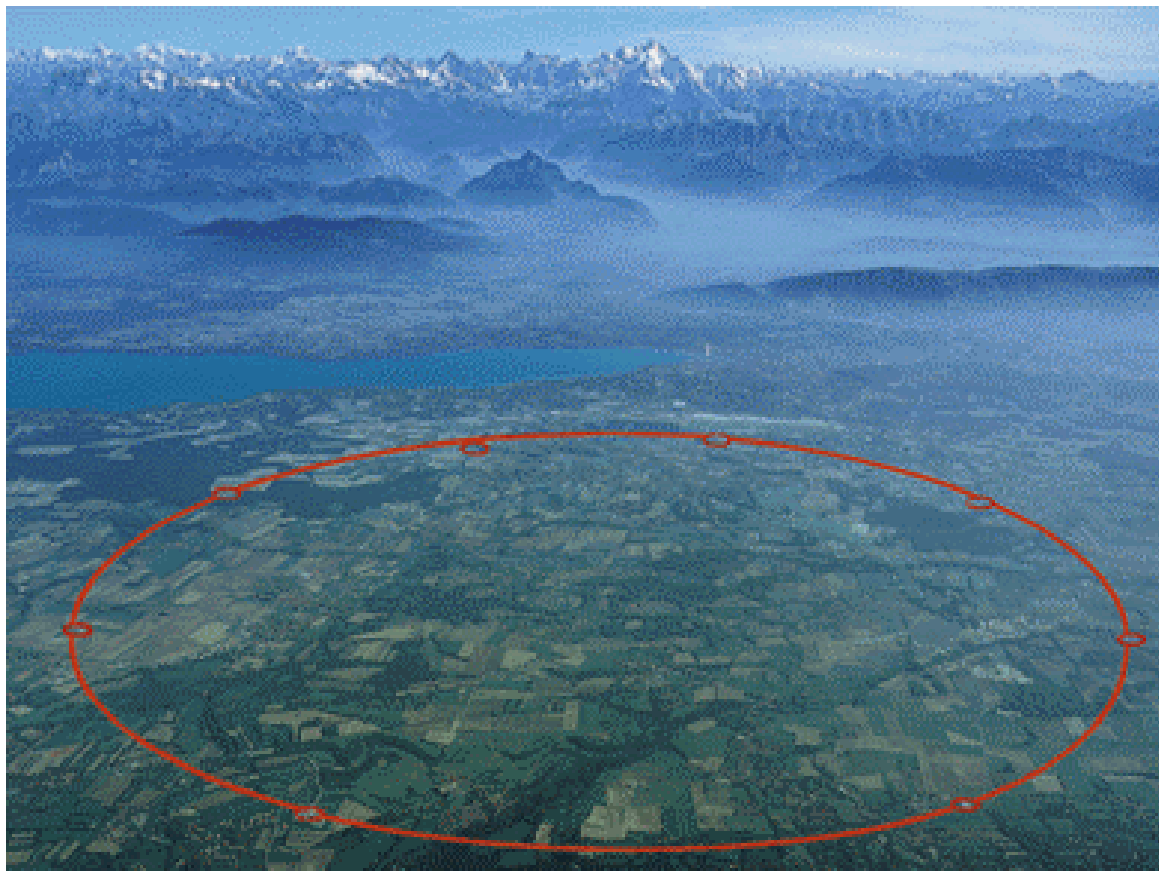
ALICE TRD Readout Electronics

Ken Oyama
Physikalisches Institut der Universität Heidelberg

Outline:

1. ALICE Experiment at LHC
2. TRD
3. TRD Readout System
   - Requirements
   - Strategy



Heavy Ion Experiments at LHC

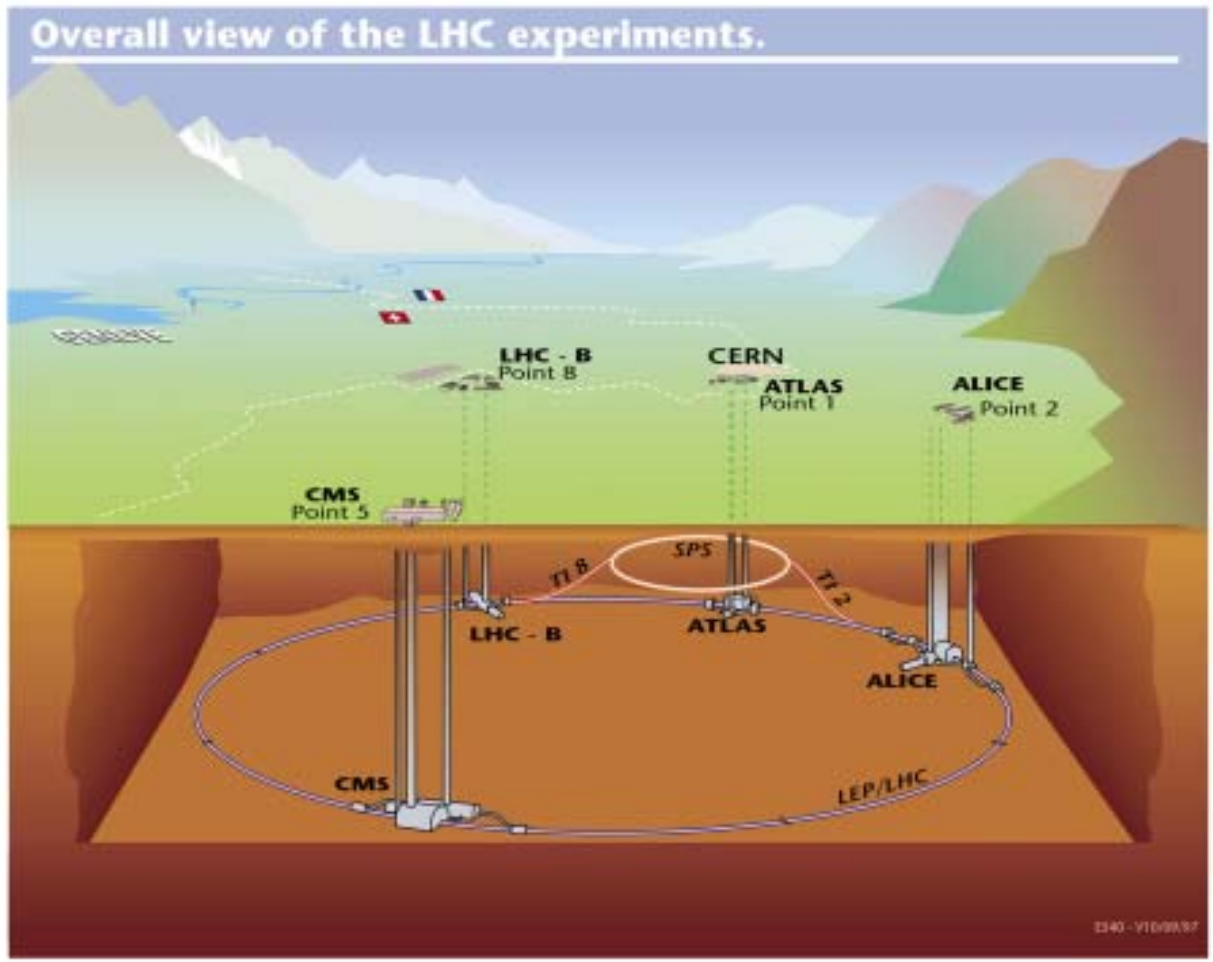
The highest energy nuclear experiment!

Pb+Pb at 5.5A TeV = 1150 TeV c.m.s. Energy

ATLAS and CMS
are considering

ALICE
is dedicated for H.I.

Our aim is : QGP study
through various proves.



Experimental conditions @ LHC

- p+p commissioning start April 2007.
- H.I. physics program at LHC

  Initial few years (1HI 'year' = 10^6 effective s)
  - 2 - 3 years Pb+Pb

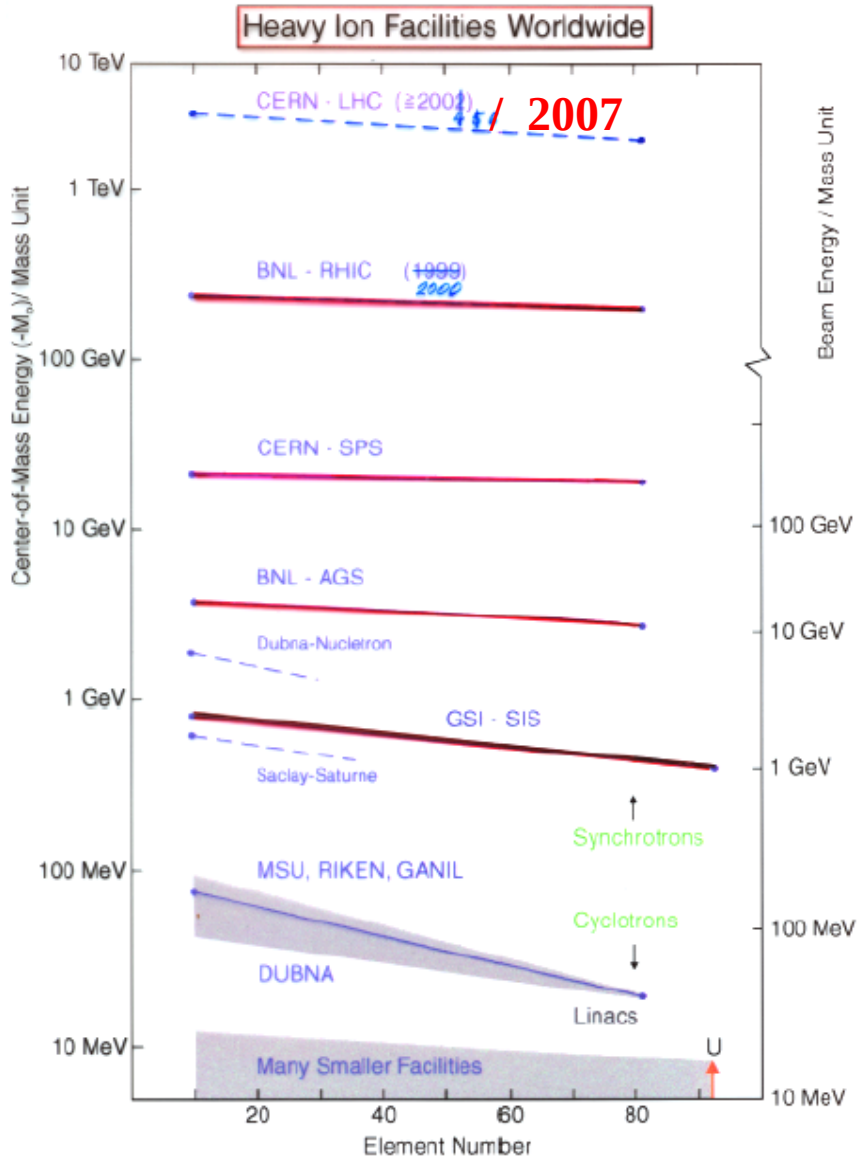
    $L \sim 10^{27}$ cm^{-2}s^{-1} (event rate ~ 8 kHz)
  - 1 year p+Pb 'like' (p, d or a)

    $L \sim 10^{29}$ cm^{-2}s^{-1}
  - 1 year light ions (eg Ar+Ar)

    $L \sim$ few 10^{27} to 10^{29} cm^{-2}s^{-1}

  plus, for ALICE (limited by pileup in TPC):
  - reg. p+p run at 14 TeV

    $L \sim 10^{29}$ and < 3x10^{30} cm^{-2}s^{-1}

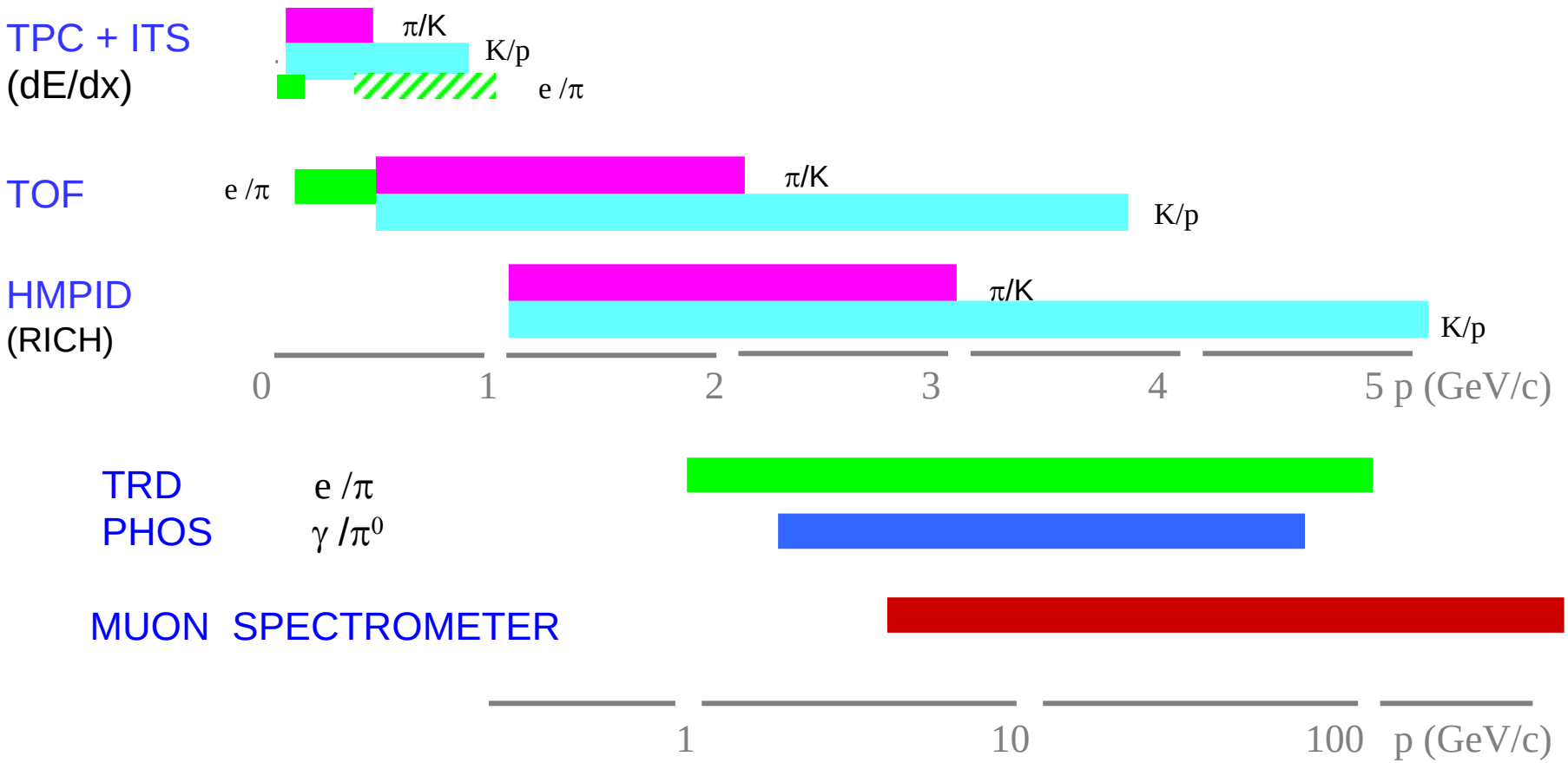


(H. Specht, QM 2001, originally from 10 years ago)

ALICE Experiment at LHC

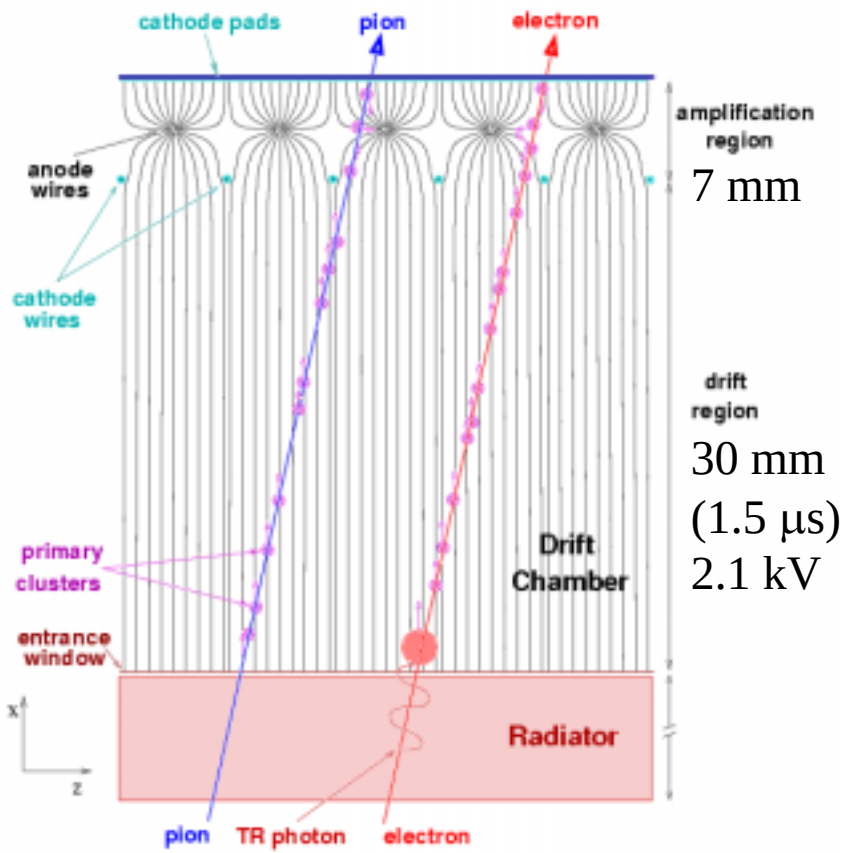
Particle Identification in ALICE

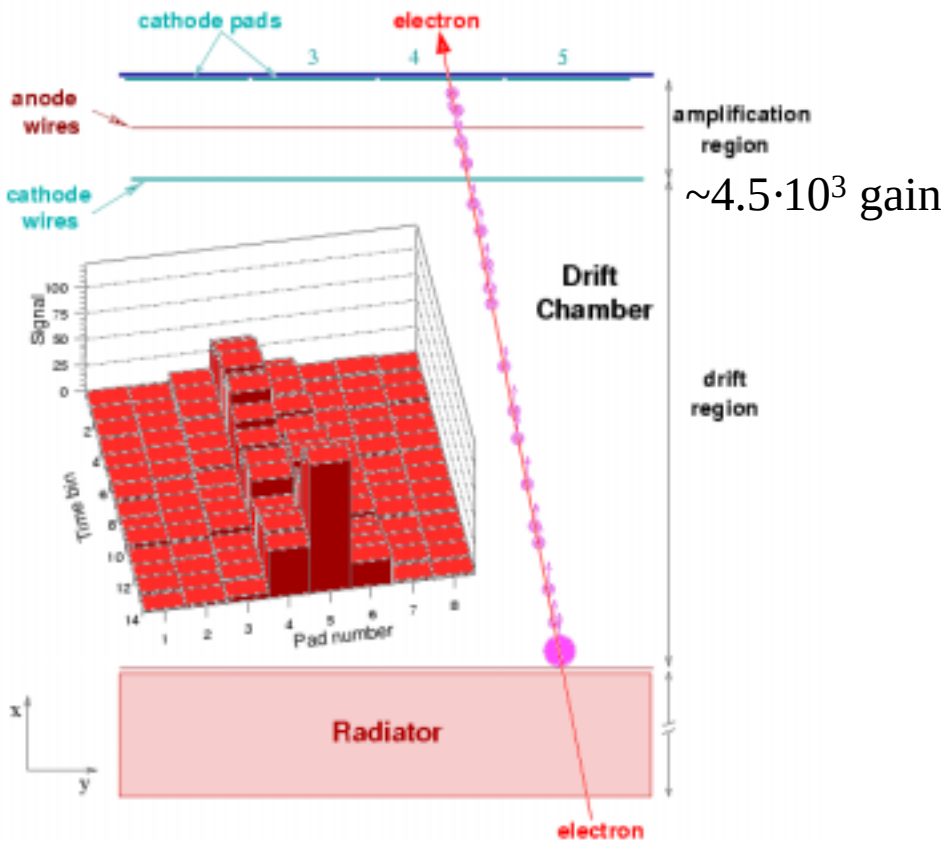
ALICE uses almost all known methods to measure low momentum to high momentum signals.



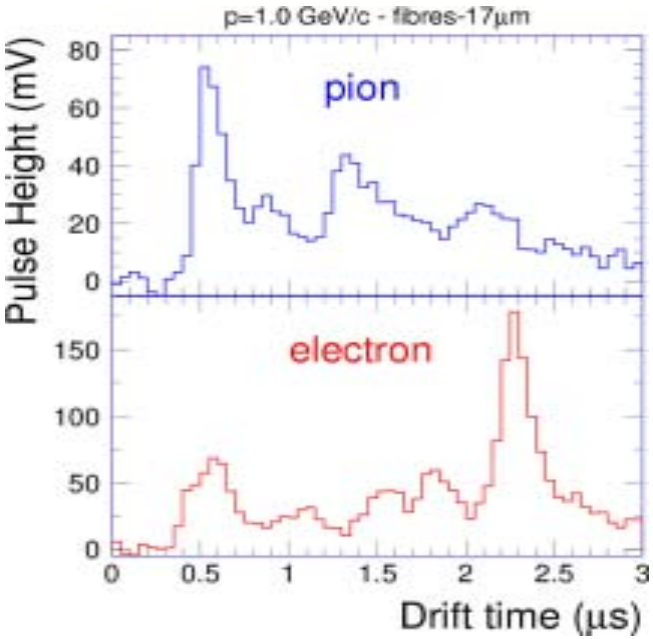
Transition Radiation Detector

- Identification of electrons at p >1 GeV/*c* and high-p_T (3 GeV/c) electron trigger.
- Principle: TR (X-ray) is emitted when a charged particle crosses the boundary of two media of different dielectric constant (**ε**). X-ray emission probability ∝ **γ**.
- X-ray is absorbed by the gas: 85% Xe + 15% CO_2.
- TRD measures both *dE/dx* and TR.



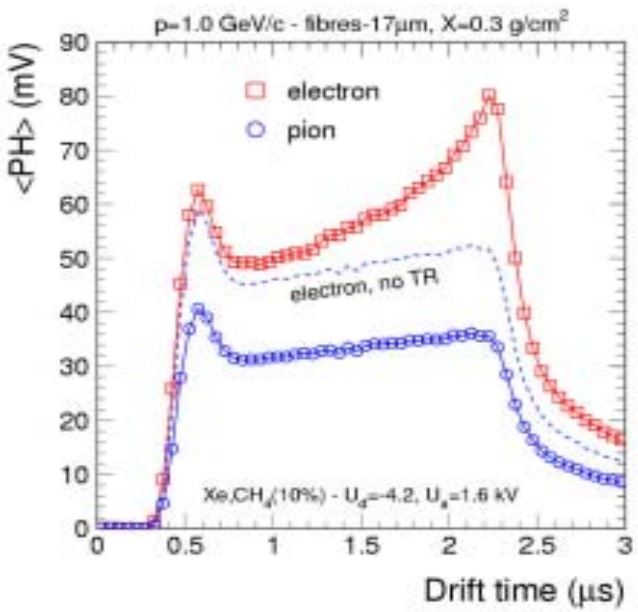


TRD signals: pions, electrons

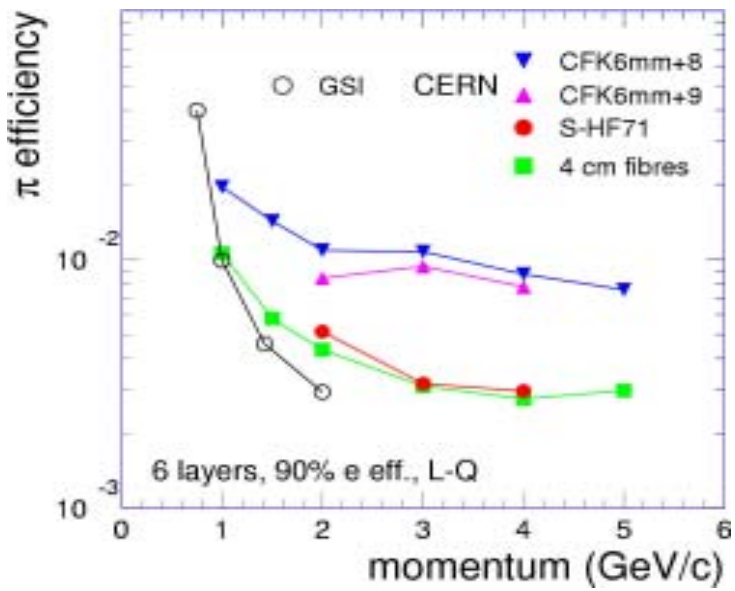


Typical response of TRD for charged pions and electrons measured by test beam experiment.

Average over many events.



200 to 300 of pion rejection factor achieved.

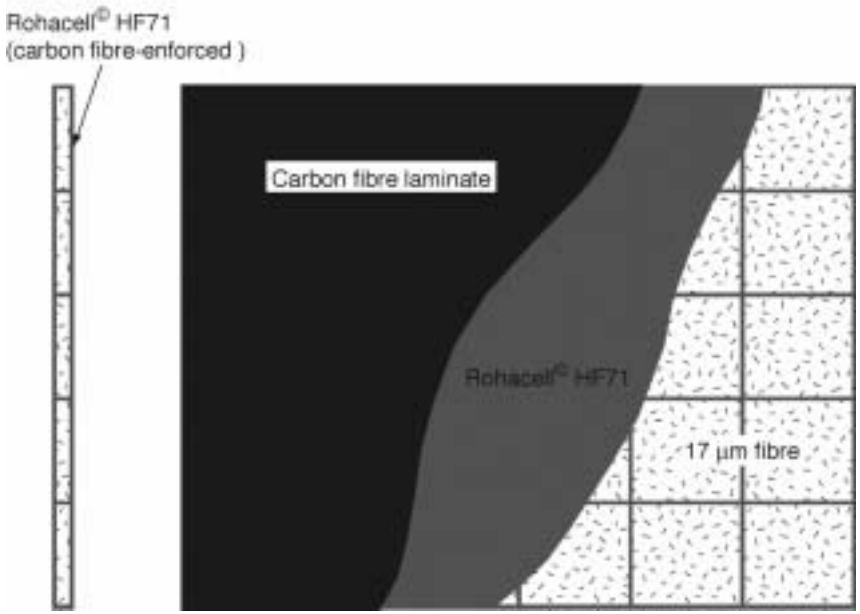


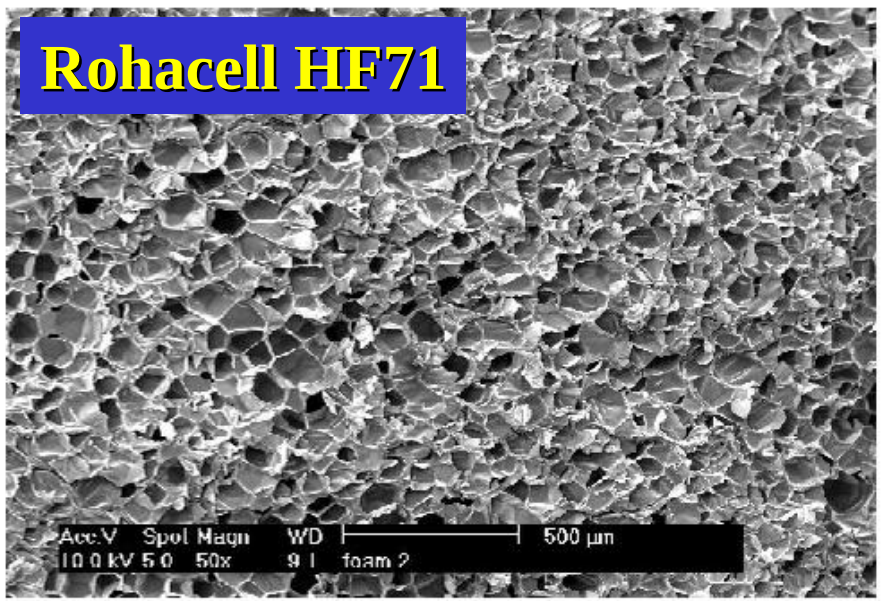
Transition Radiator

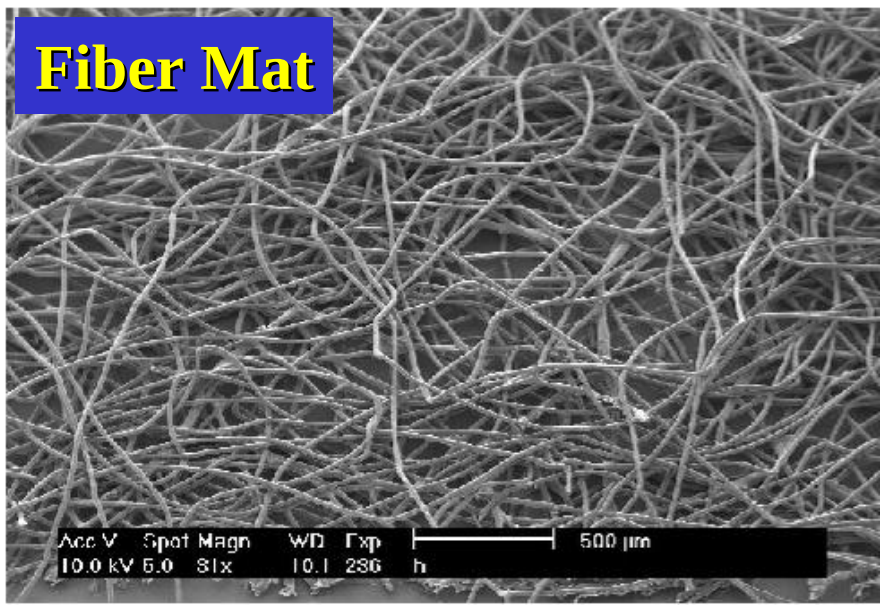
Sandwich of:

- **Rohacell HF71**
  - **(with carbon fiver enforced)**
- **Polypropylene fiber (17 μm)**
- **Air**

Thickness total 48 mm.

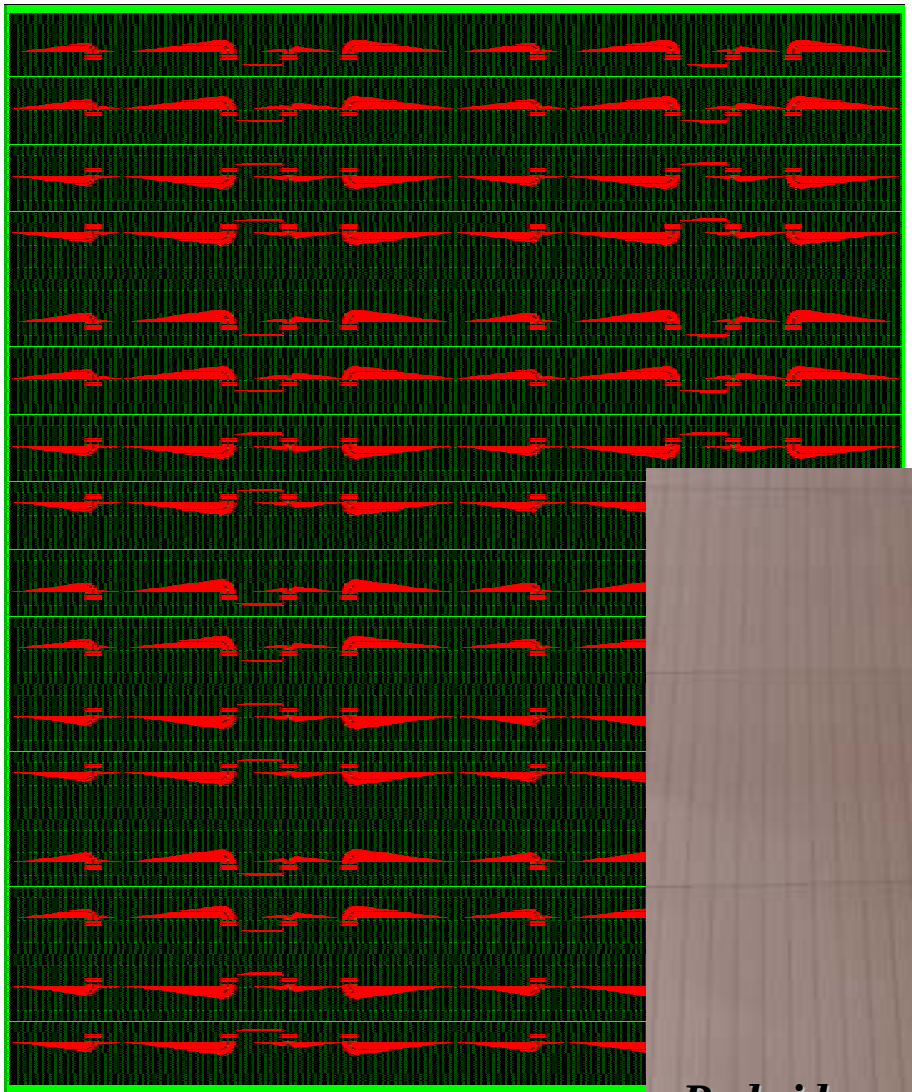


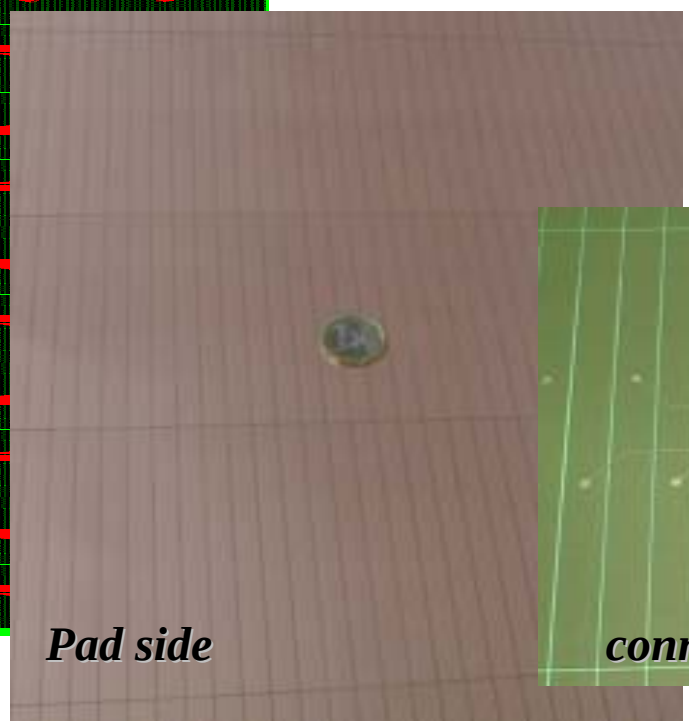


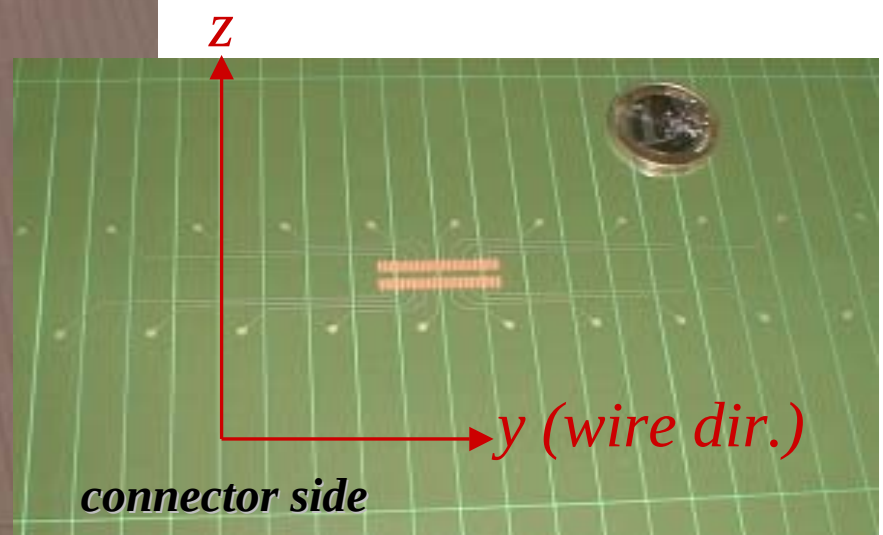


Padplane Prototype

- Huge printed circuit boards, made of thousands of ~ 7 x 80 mm^2 pads, each one sheared by an angle of 2 degrees.
- Pos. resolution $r\Delta\phi$ = 0.04 mm, Δz = < 1 mm
- 0.36 mm thick halogenefree FR4 coated with 17 μm copper.
- Pads on one side, on the opposite side traces running to cable footprints,
- Grouping each 18 pads.

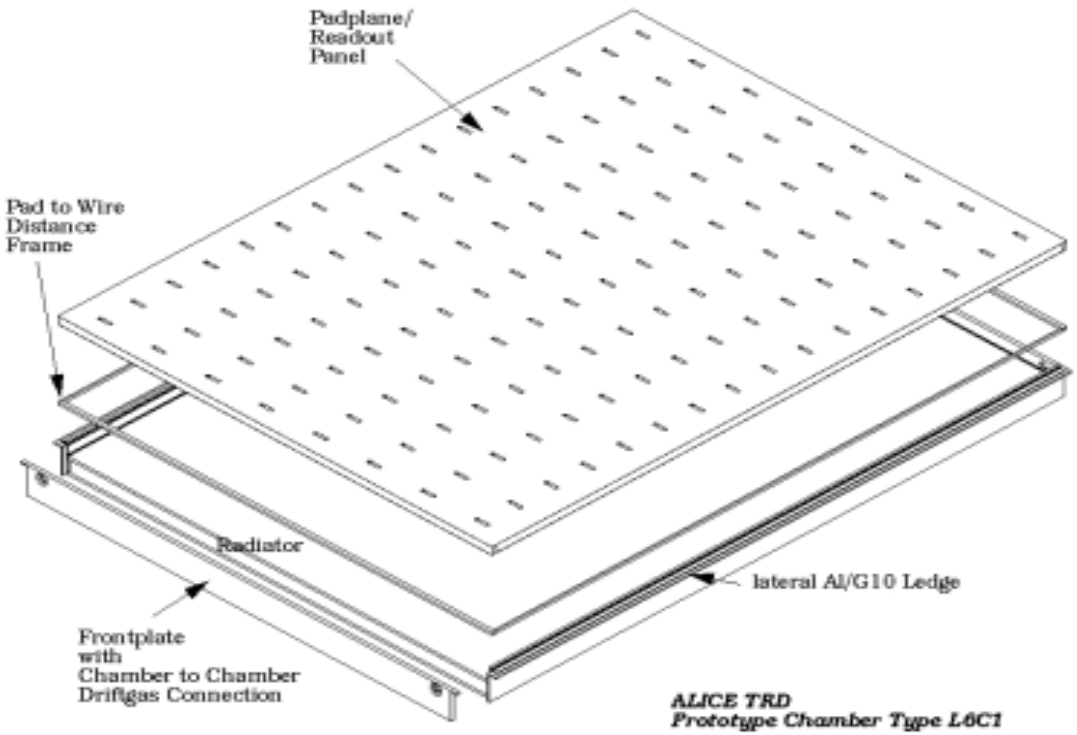






Full Size Prototype Chamber

Pad- Readout Panel **-> INVENTOR (Krakow)**
-> PI Uni Heidelberg (cutouts, glueing of pad planes)
Radiator **-> INVENTOR (panels)**
-> IKP Uni Muenster (assembly)
Main frame, wire ledges, etc. -> PI Uni Heidelberg (production and assembly)



<u>Three main production steps:</u>

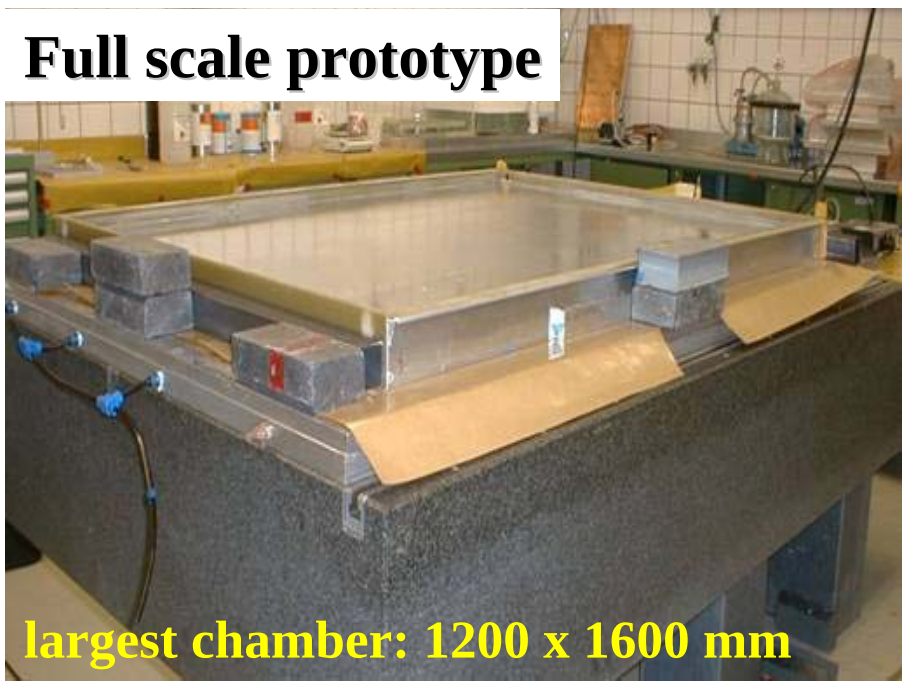
- **glueing main frame to radiator**
- **electrical connections and applying the wire planes**
- **closing the chamber with pad-readout panel**

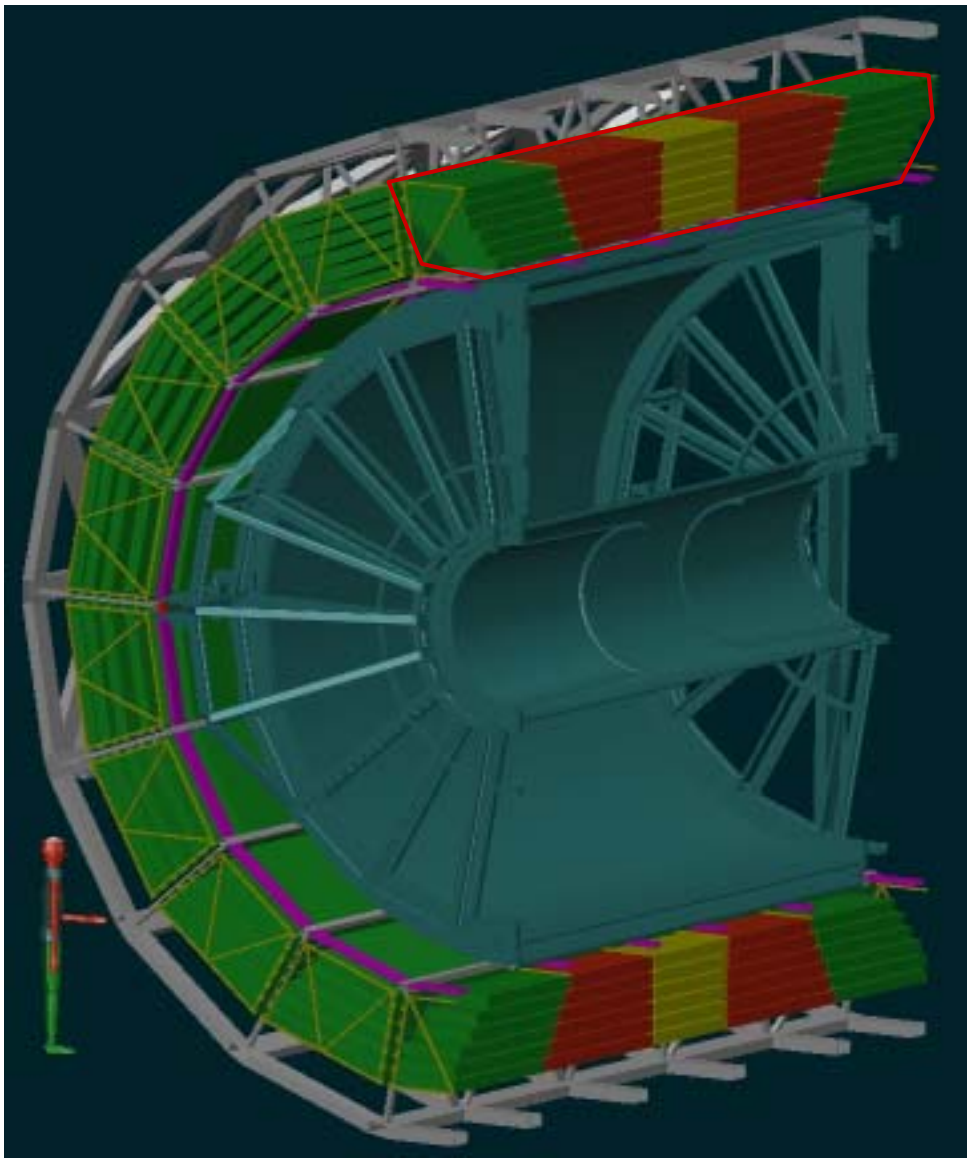
Construction

540 chambers are combined into barrel shape space frame subdivided into 18 supermodules.

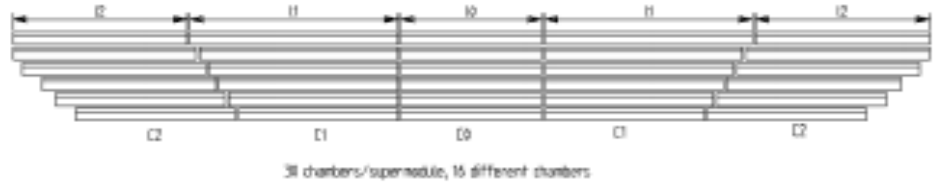
TRD covers 360° azimuth and $-0.9<\eta<0.9$.

The full TRD has (4 * 16 + 12) * 144 * 6 * 18 = **1,181,952** individual channels, it's the worlds biggest TRD with an active area close to the size of 4 tennis courts (751 m^2).

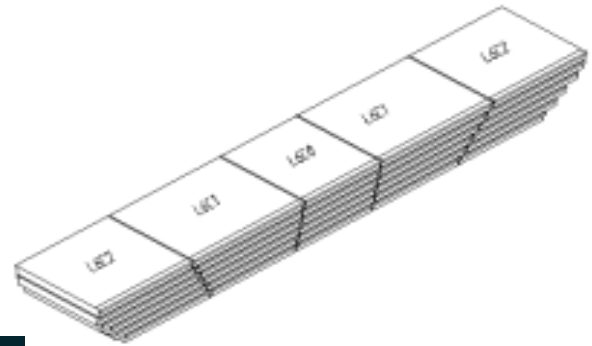




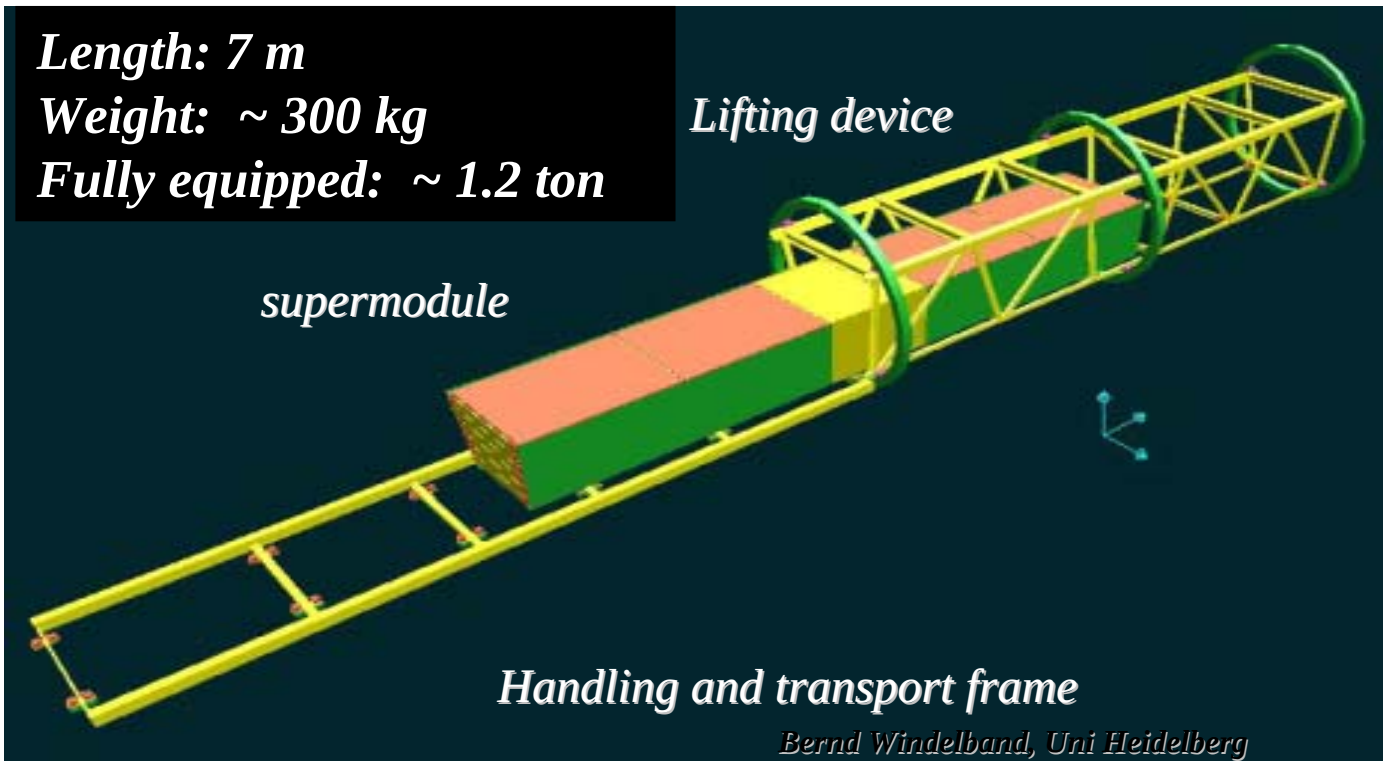
Supermodulalization



16 different types of chambers
Min. 1080mm x 974mm x 105mm, type L1C0
Max. 1585mm x 1196mm x 105mm, type L6C1

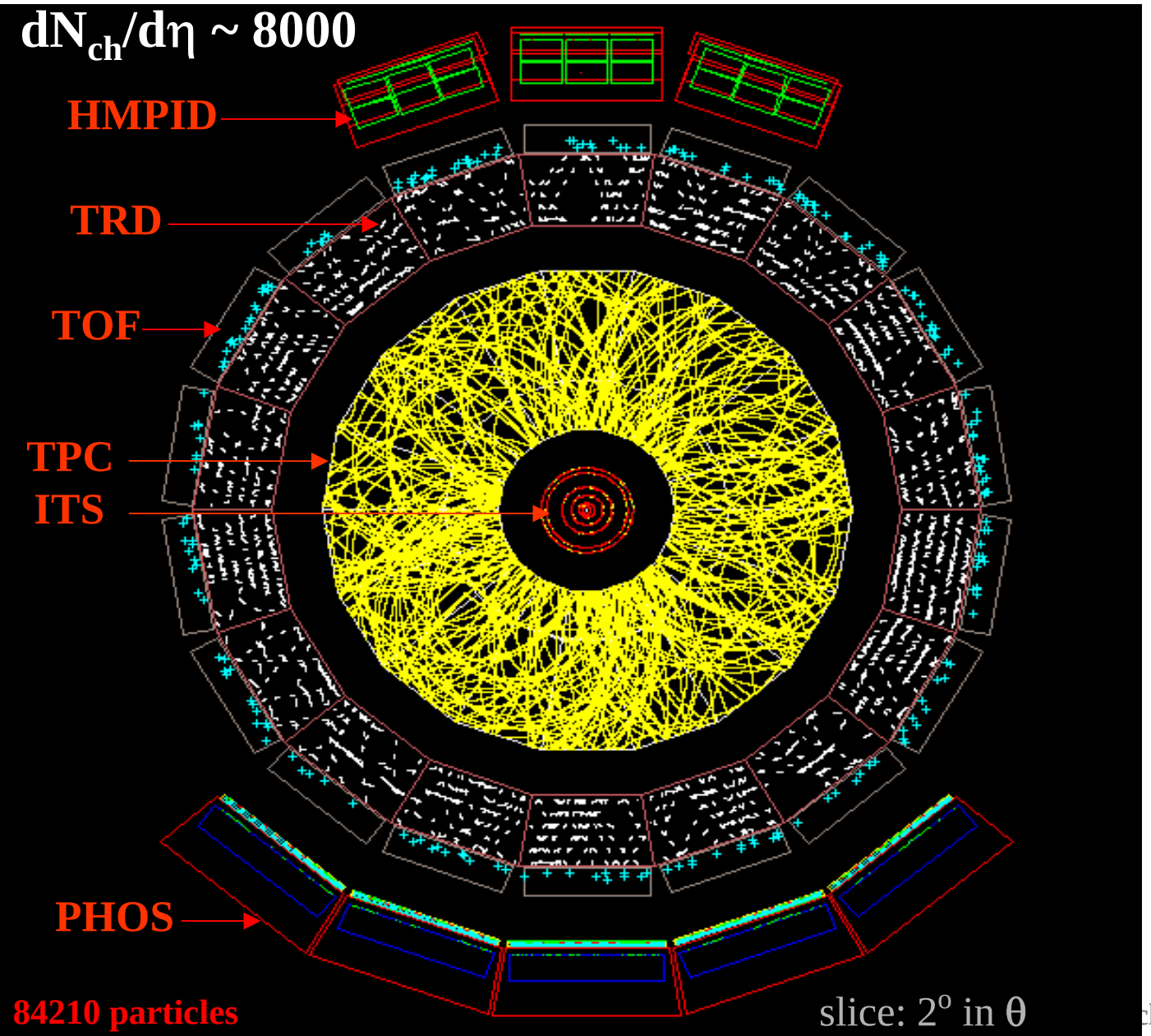


ALICE-TRD, overview of different chambers in one supermodule



6 x 5 = 30 chambers are combined to 1 big supermodule.

ALICE Performance Requirement



Expected:

dN$_{ch}$/dη ~ 8000

TPC/TRD should accept:

20000 primary charged particles.

Simulation:

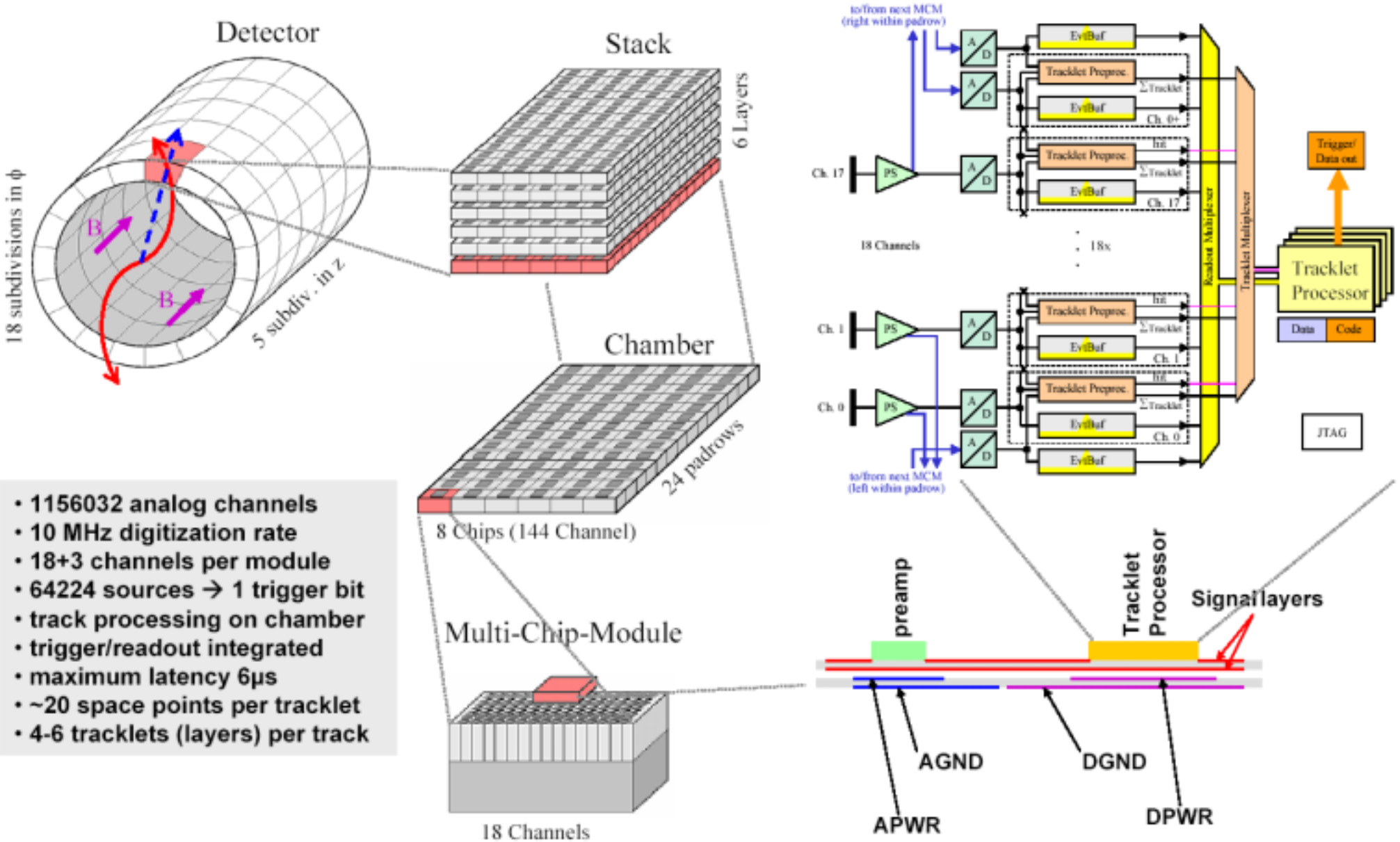
Event data size

- Hits ~ 1.4 GB
- Digits ~ 1.1 GB

CPU time on 800MHz PIII

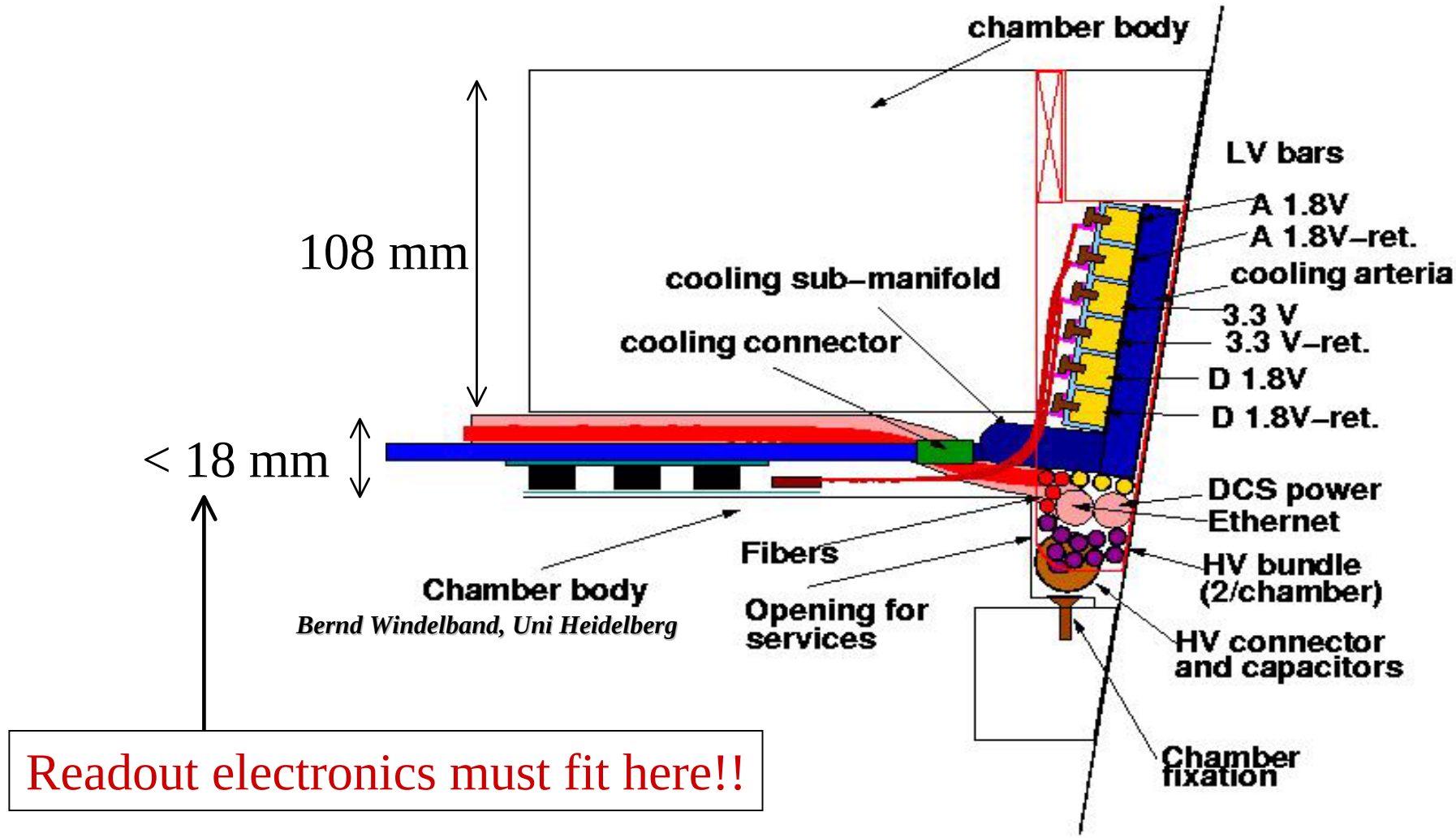
- Hits ~ 24h
- Digits ~ 15h

TRD Readout System - Strategy and Requirements



- 1156032 analog channels
- 10 MHz digitization rate
- 18+3 channels per module
- 64224 sources → 1 trigger bit
- track processing on chamber
- trigger/readout integrated
- maximum latency 6μs
- ~20 space points per tracklet
- 4-6 tracklets (layers) per track

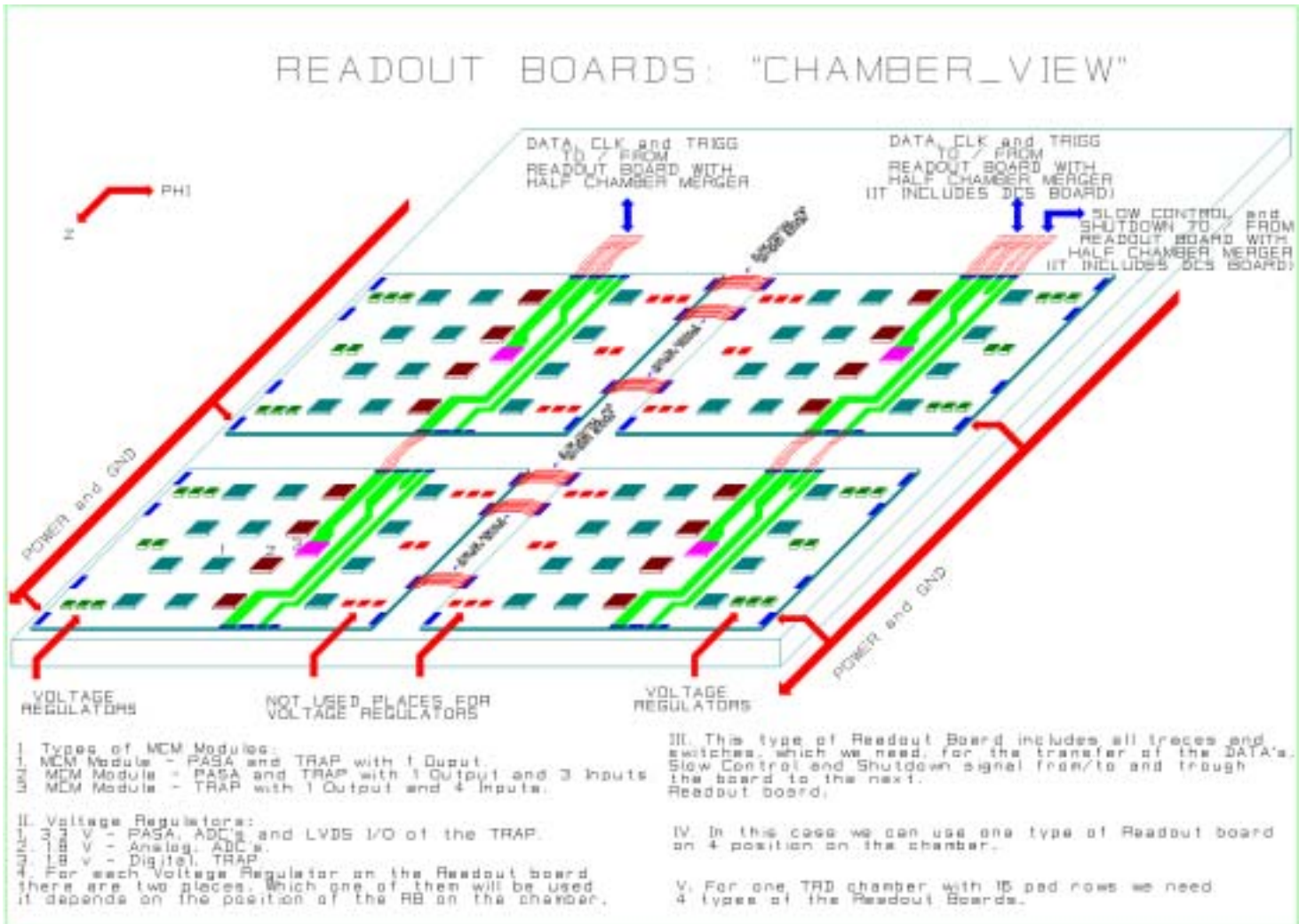
Limited Space in Supermodule



Power consumption < 50 mW/ch (50 kW total)

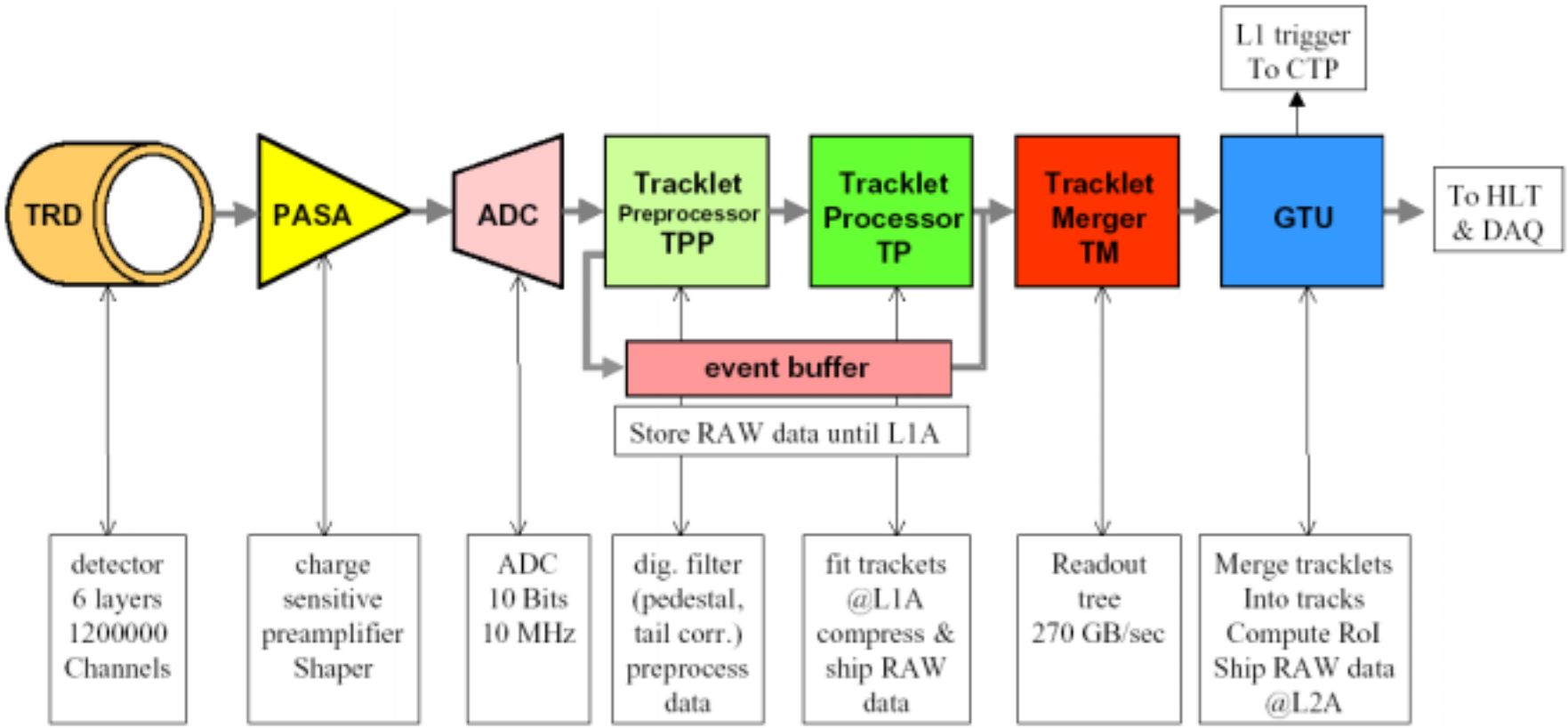
Readout Board

0.6mm thickness, 4 layers PCB
4×4 Multi Chip Modules (MCM).
Water cooling.

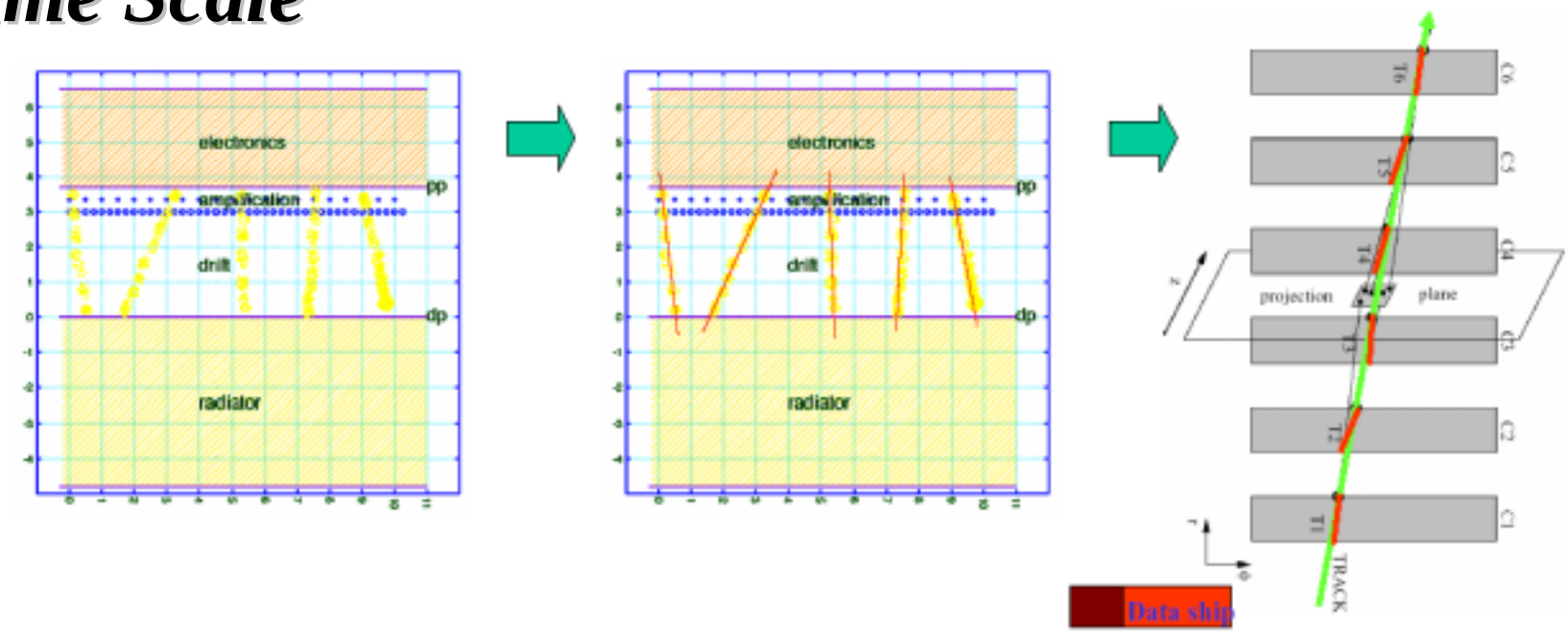


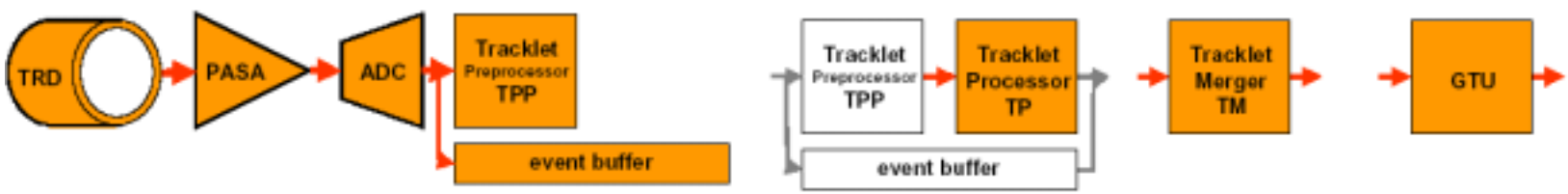
TRD Readout System – Data Flow

- Develop and analog/digital mixed custom LSI.
  1. Preamplifier and shaper chip (PASA).
  2. ADC and digital processing chip (TRAP).
- GTU (Global tracking unit) massively parallel **FPGA processor → Level 1 trigger**.
- **TRD data flow rate at ADC : 14.5 TB/s (30 MB / event).**



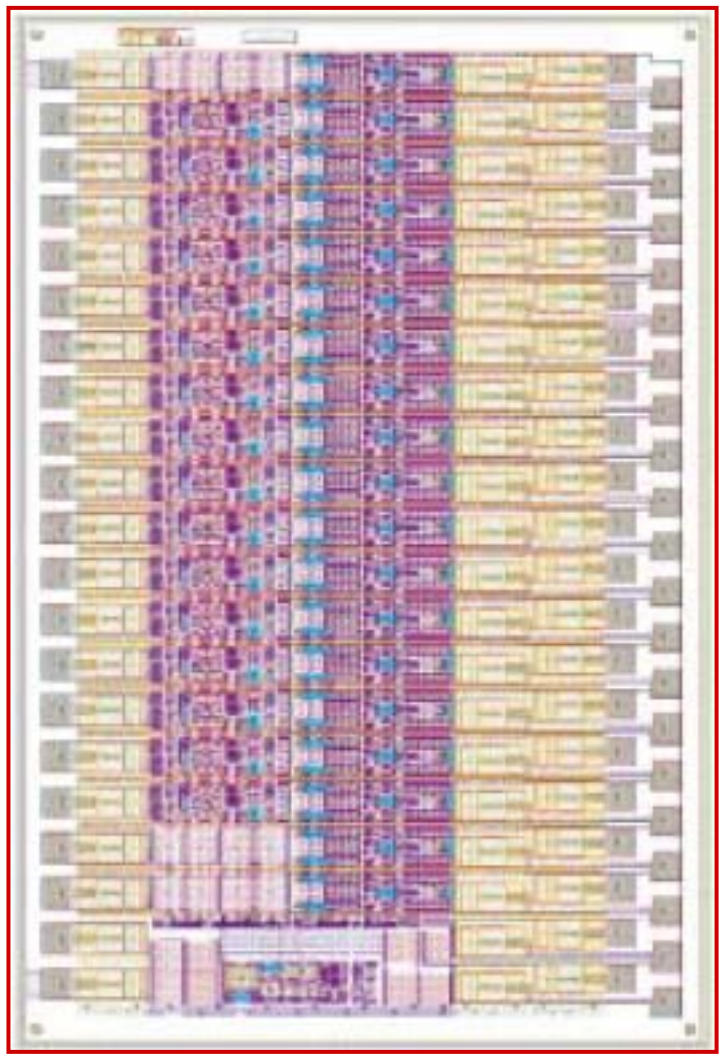
Time Scale


electronics
amplification
drift
radiator
pp
dp
projection
plane
TRACK
Data ship
Calculate Σ fit
Calculate Tracklets
relevant pipeline ADC output
Global Tracking
Drift time
998
1996
2994
3992
4990
5990
t [ns]

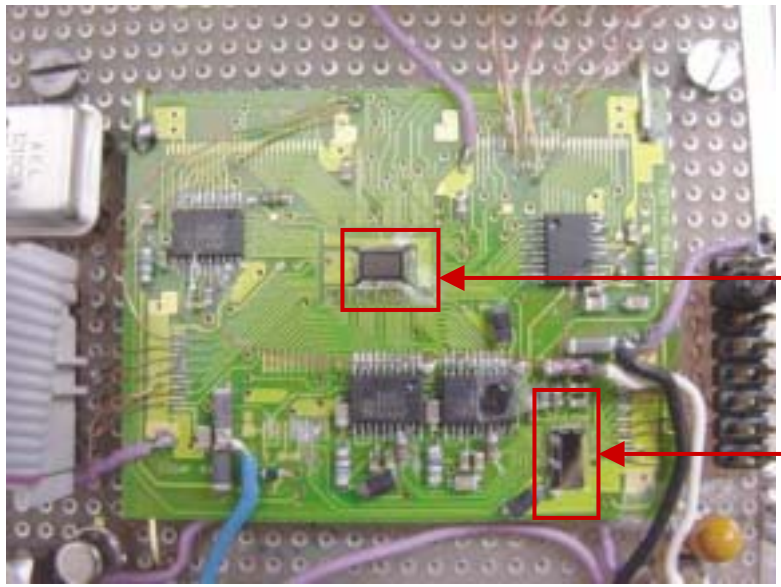

TRD
PASA
ADC
Tracklet Preprocessor TPP
event buffer
Tracklet Preprocessor TPP
Tracklet Processor TP
event buffer
Tracklet Merger TM
GTU

PASA (Preamplifier and shaper chip)

- 18 ch. preamplifier and shaper
- 350 nm technology
- 12 mV/fC gain
- Noise: 1000 *e*
- Shaping time 120 ns
- Cross talk < 0.3 %
- Max power consumption < 10 mW
- Input dynamic range 164 fC.
- Output pulse level 1V.

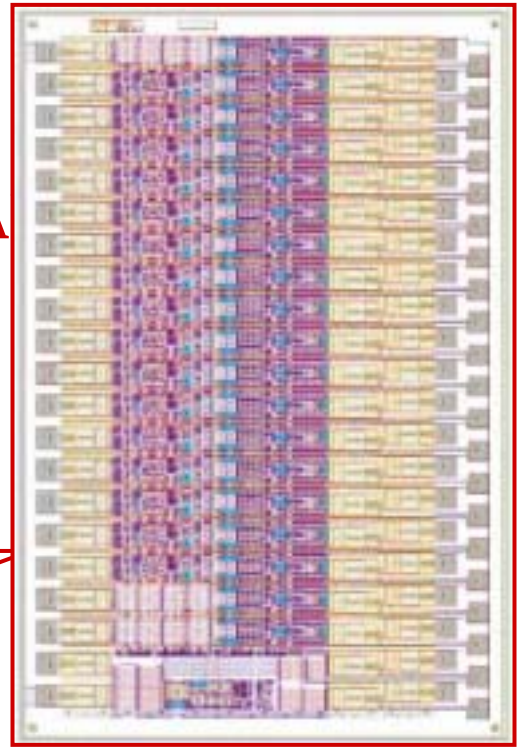


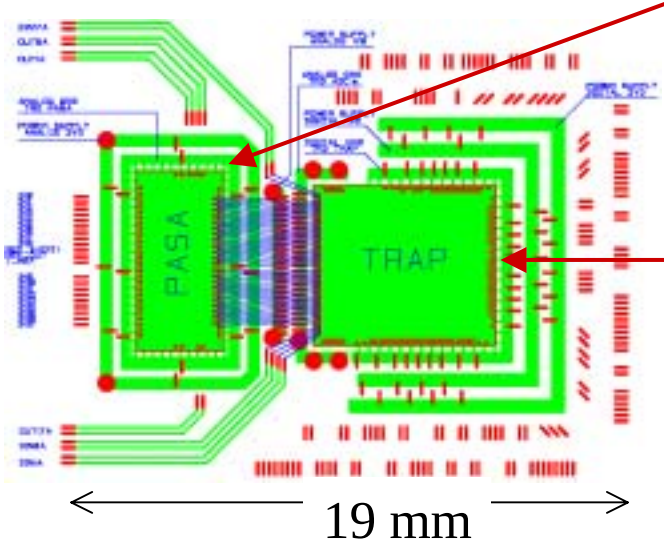
MCM Prototype and Final Design



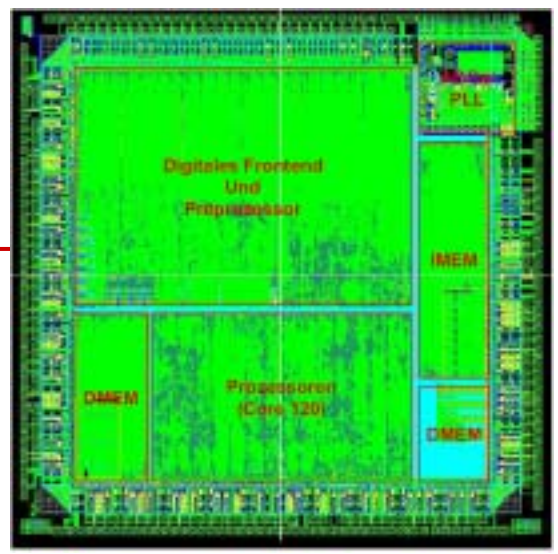
Prototype TRAP
without ADC

PASA



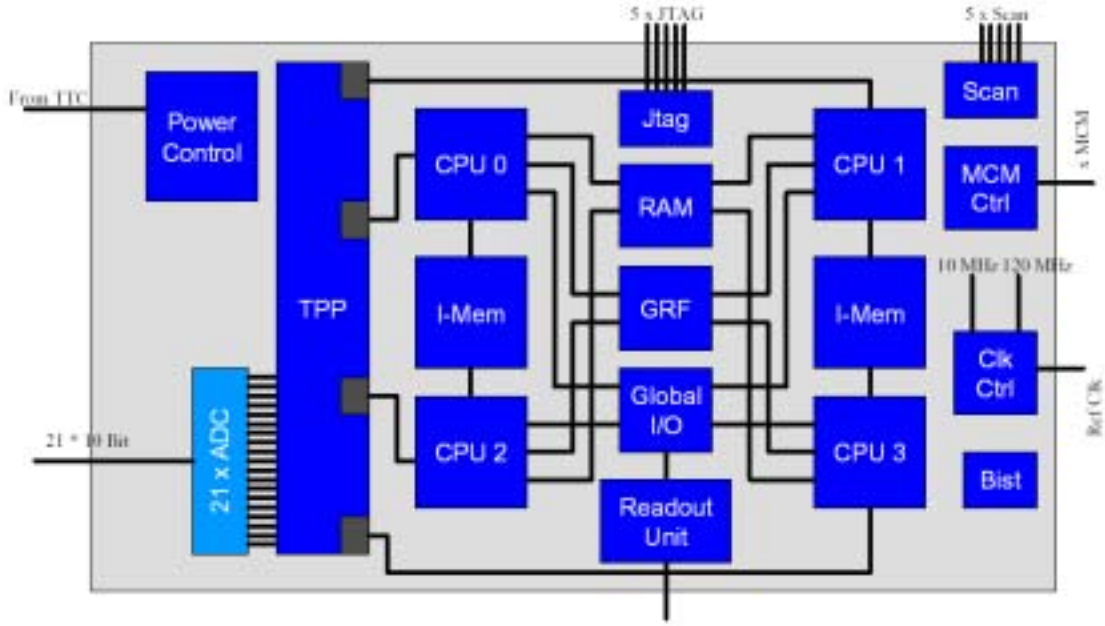


TRAP



TRAP Chip

***KIP** people are working for it.*



Includes ...

21 ch. ADC:

10 MSPS, 10 bits, 1 clock latency.

< 1.5x1.5 mm^2 die size.

6 mW/channel.

TPP (Tracklet preprocessor):

Digital filters.

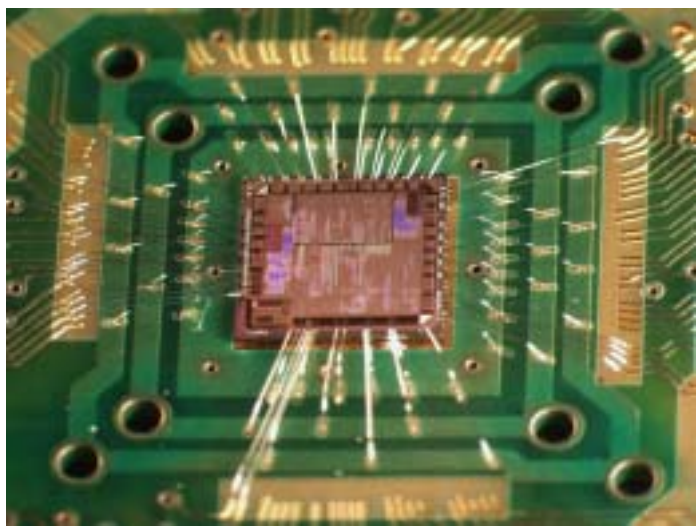
Continuously summing data for TP.

Event buffer: Store data.

TP (Tracklet processor):

four 120 MHz RISC MIMD processors

Communication using quad port memory (full custom).



April 2002 TRAP1 (1st prototype)

120 nm process with 4.5 M transisters.

Digital Filter and Local Tracking in TRAP

■ **Digital filters** are implemented in the TRAP chip.

1. Tail cancellation filter
2. Pedestal correction
3. Cross talk filter

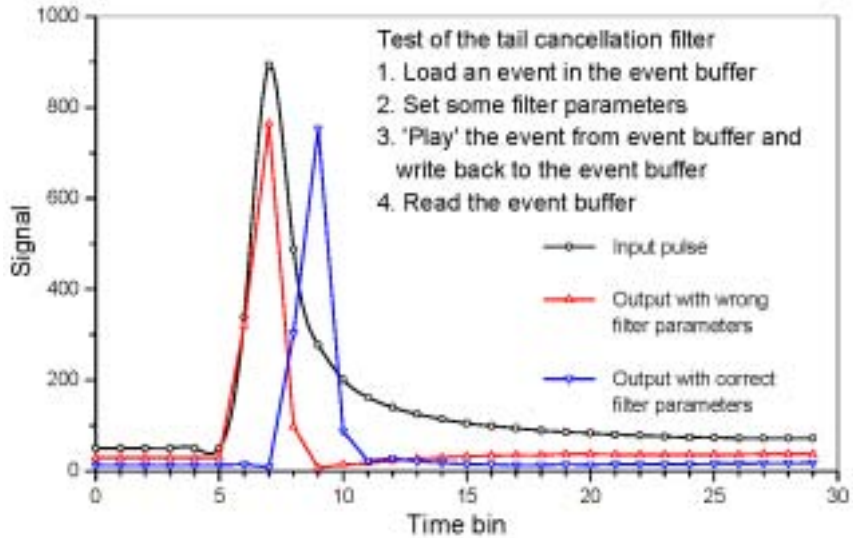
■ **Primitive sums** for fitting stage.

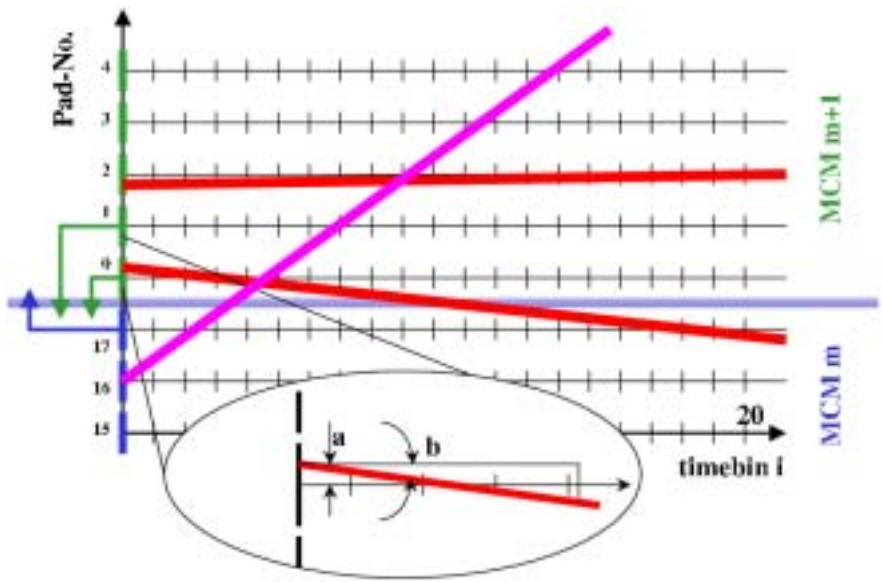
■ **Detector local tracking**.

Straight line fit:

$y_i = a + b\,x_i$

(40 tracklets per chamber)





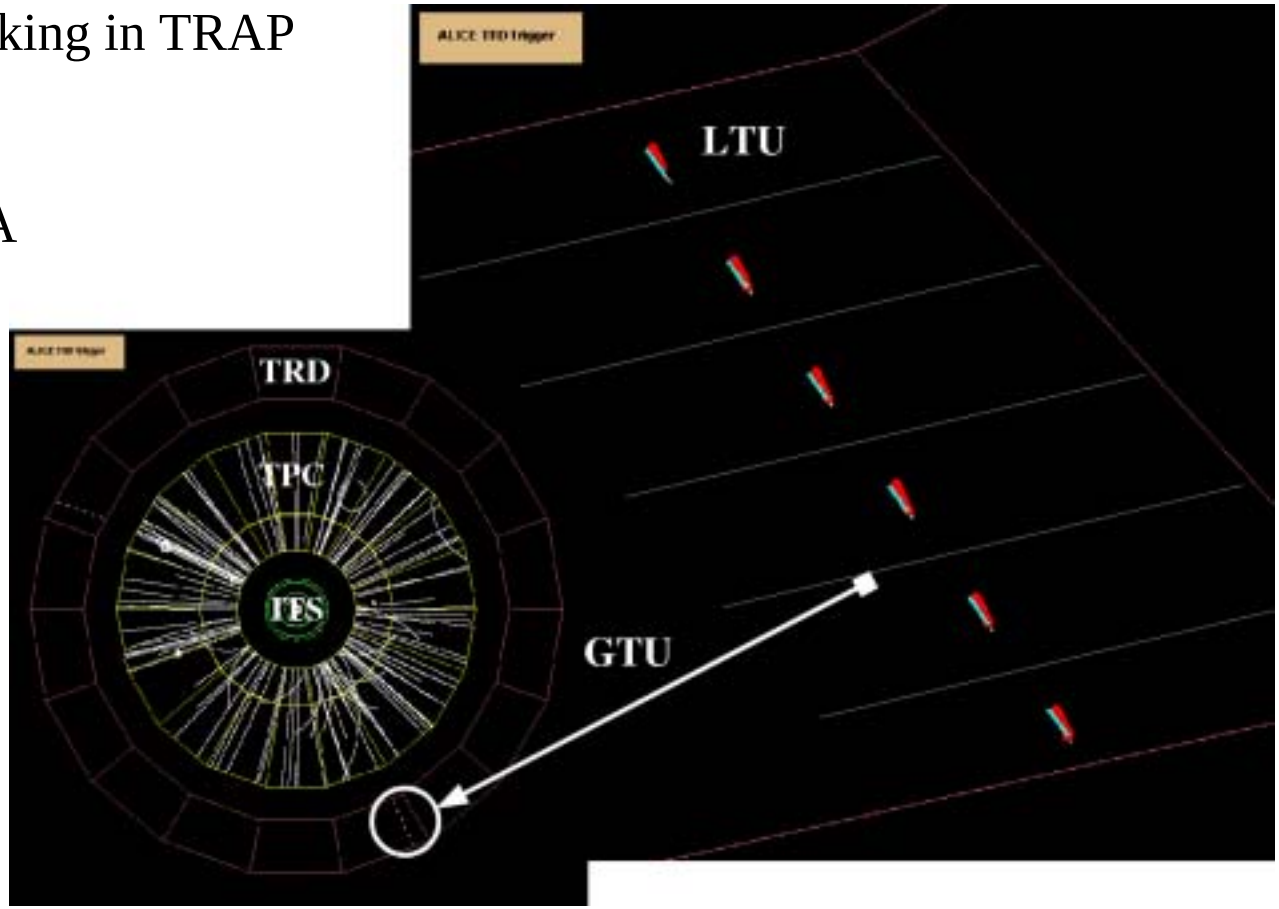
Local Tracking to Global Tracking

LTU Result : Detector local tracking in TRAP

⇩

GTU : Global Tracking on FPGA

Combine tracklets.
Momentum reconstruction.
Pair reconstruction
(mass and p_T).

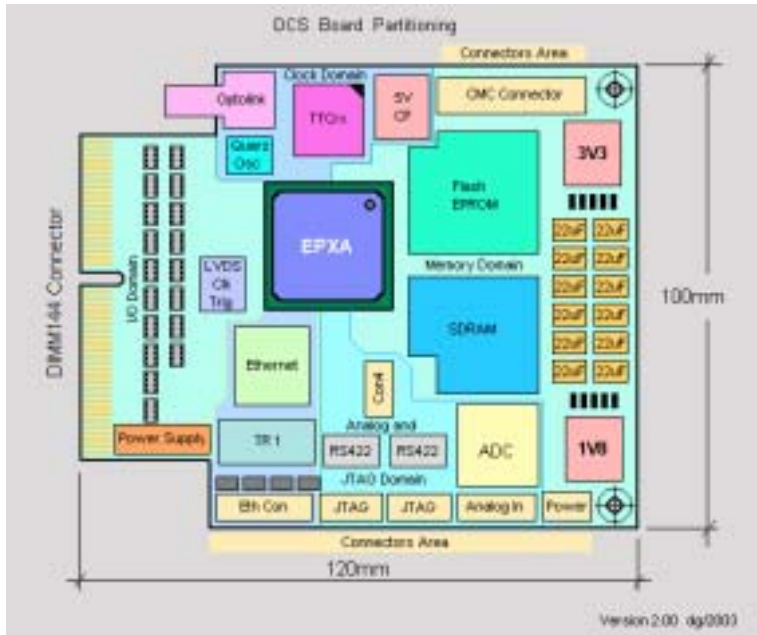


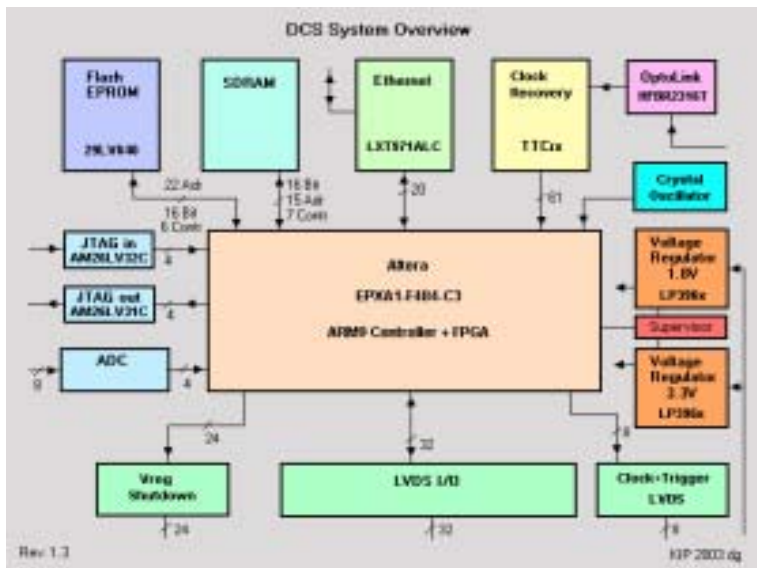
C++ & GEANT → Floating → nearly infinite digits.
FPGA → Non floating → finite digits. → **~ 8 % worth** resolution
Difficulty of response simulation and porting each other. Still being studied.

DCS (Detector Control System) Board

- Limited size: 100 x 120 mm.
  Height: 10.5 mm max..
- First prototype April.
- Altera 100k gates FPGA flexibility.
- ARM core in FPGA.
- 32 MB RAM / 16 MB flash ROM.
- LINUX system on FPGA.
  a chamber = a Linux PC with 100 Base-T ethernet.
- TTCrx clock recovery.
- RS422, JTAG.
- LVDS clock & trigger driver.
- 16(24) bit ADC with 10 SPS.

- Design freeze.
- Prototype made and now Linux booted.





Conclusions

■ ALICE TRD project has many challenging technologies:
Online tracking using full custom analog/digital mixed LSI (PASA and TRAP).
MCM.
Custom FPGA-Linux based intelligent control system (DCS).

■ Prototype test of MCM is done and final design MCM is now being developed.

■ We are testing prototype DCS board.

■ Chamber production: design is almost fixed. Started purchasing materials.