# A Fast DAQ Front End for Photon Counting using an FPGA

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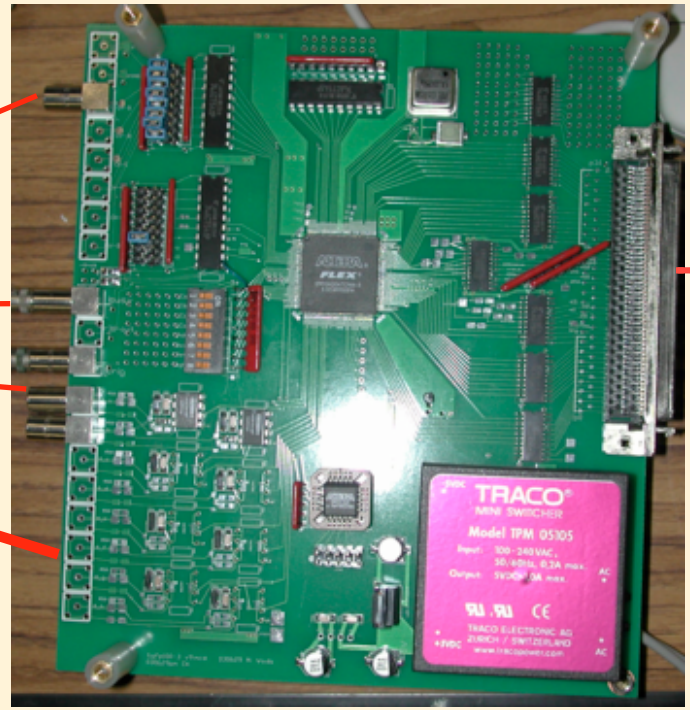
**Top Performance with Minimum Time, Skill, Cost,...**

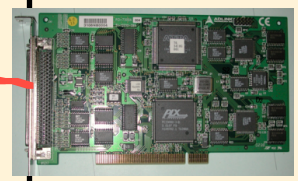
0~40 kevents/s
analog ~4 ch
tag ~4ch

Circuits

Detector




a PCB with an FPGA
and 8 ADC



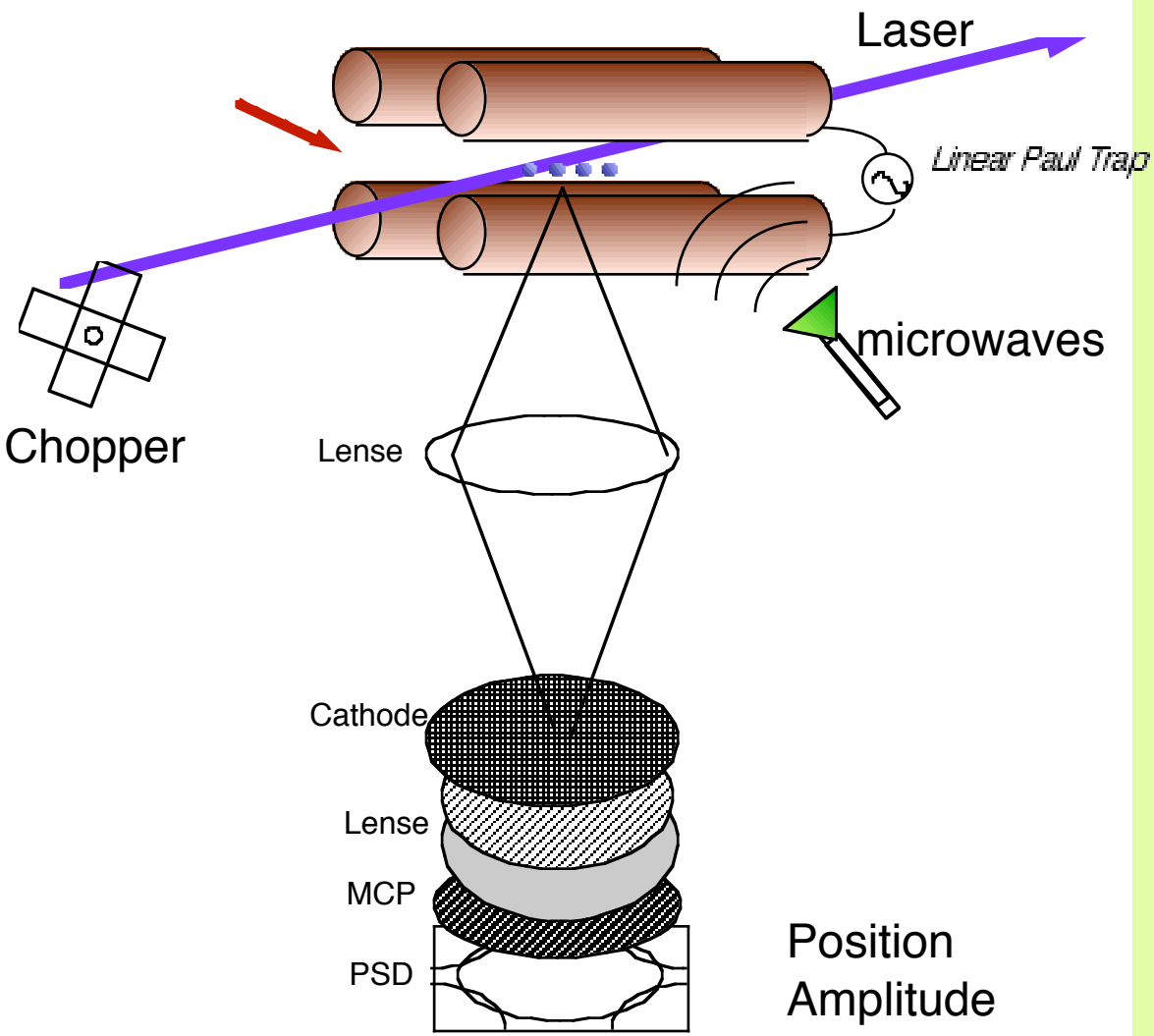
32bit DIO
with FIFO

PC RealTime Linux
(RTAI)

PC
GUI
LabView

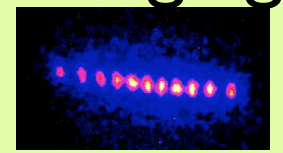
*Experiment:*

# Laser Induced Fluorescence Spectroscopy for Trapped Ions




Position Sensitive Photon Detector
PIAS-TI

- Imaging Ion Crystal



Commercial DAQ works

- HFS Spectroscopy

additional Tag Data

*microwave frequencies
*time since laser pulse
*time since microwave pulses
*etc

in Event by Event DAQ

Event Size

~10 words(16bit)

Event Rate

max 10^8 photon/ion/s
ϵ=~10^-4
R=0~40 kcps (detector limit)

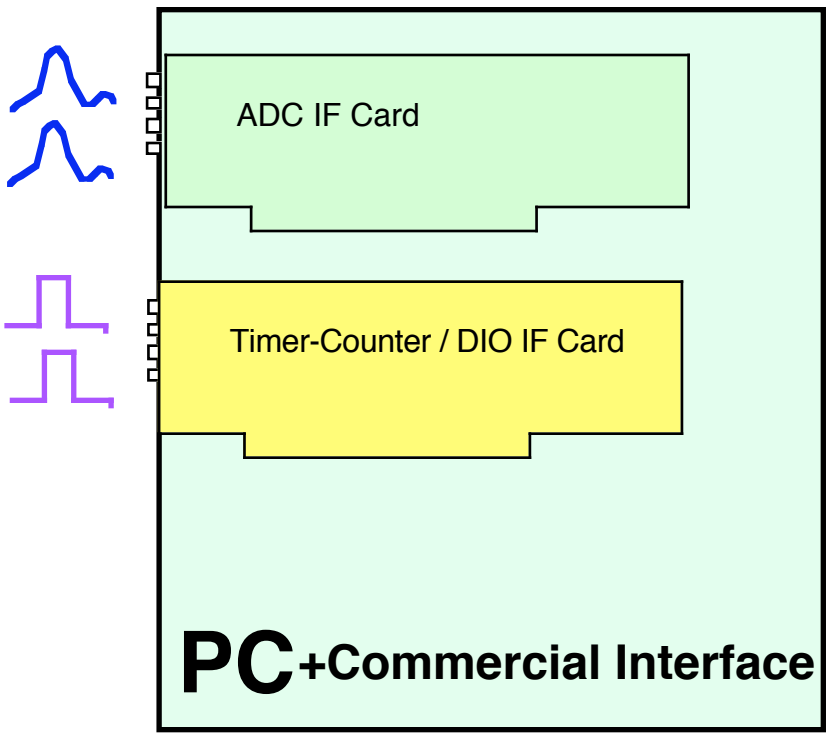
Dead Time

20 s : ~80% useless
2 s: ~8% acceptable

Throughput

< 1 Mbytes/s : moderate

# Event by Event Interrupt




**Trigger -> Interrupt**

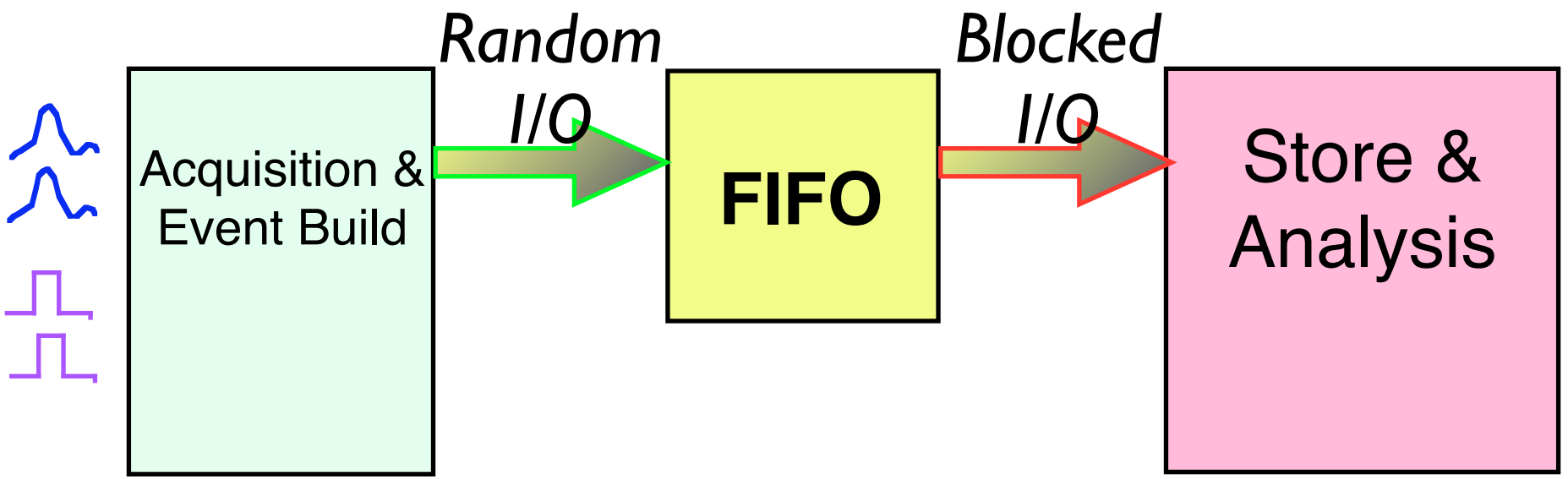
```
Interrupt Service Routine()
{
    Latch Counters;
    Latch DIO;
    Read ADC Data;
    Store Data into Ring Buffers;
}
```

**Dead Time: > multi 10s s**

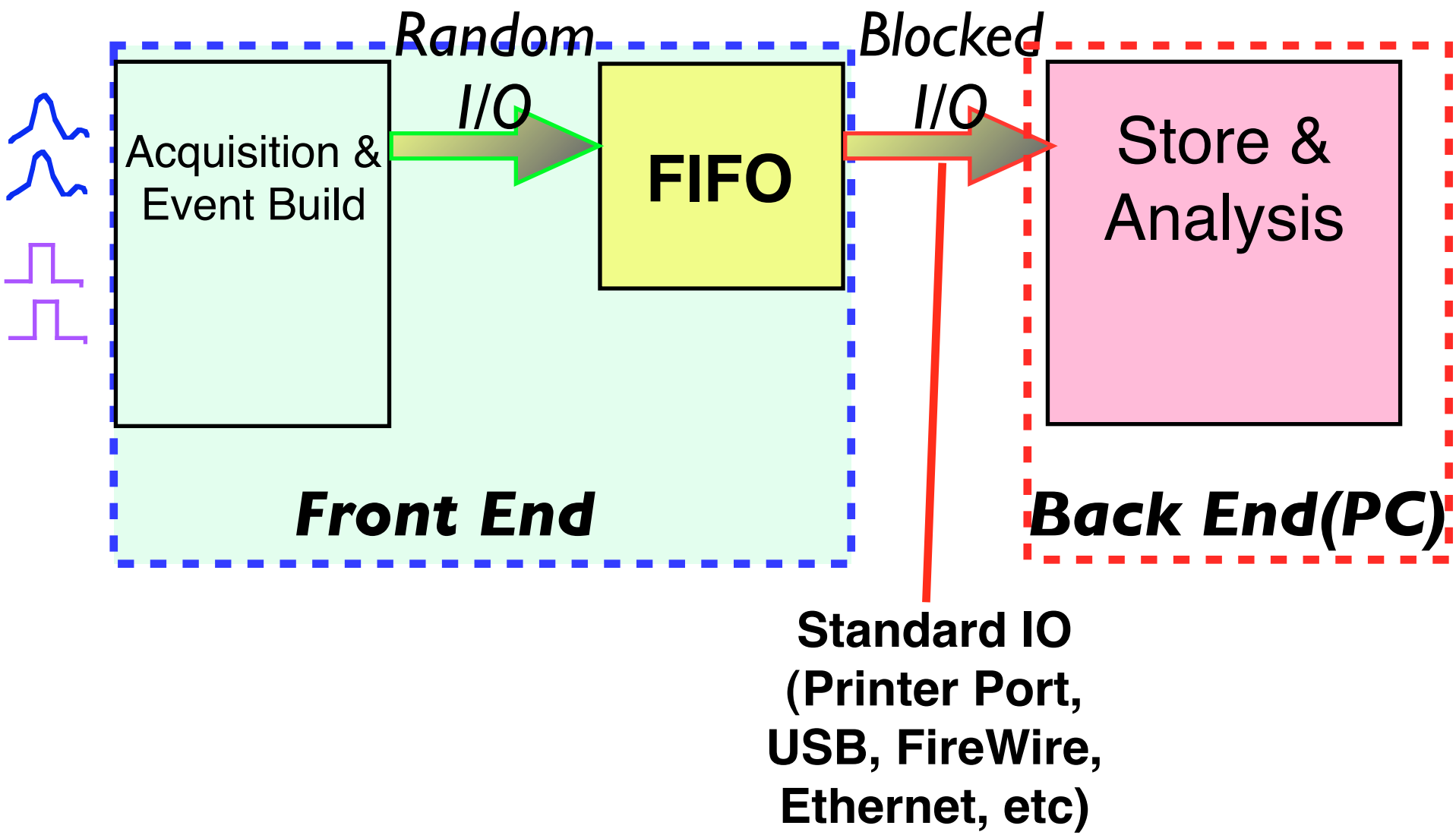
**∴ Event/Event Acquisition must be done by Hardware**

**Throughput 1Mbyte/s：**
**Quite Easy for Modern CPU and Hard Drive**

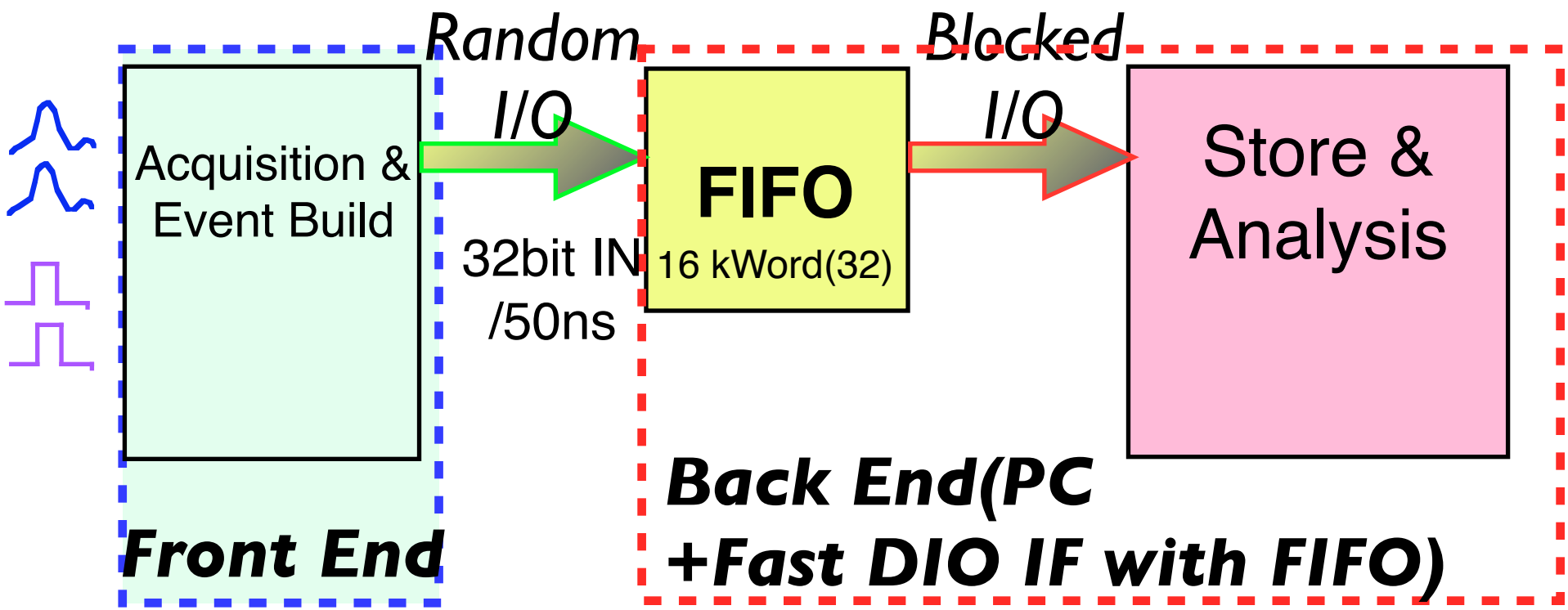
# Buffering Model



# Buffering Model -1



# Buffering Model -2




*Very Simple Architecture*

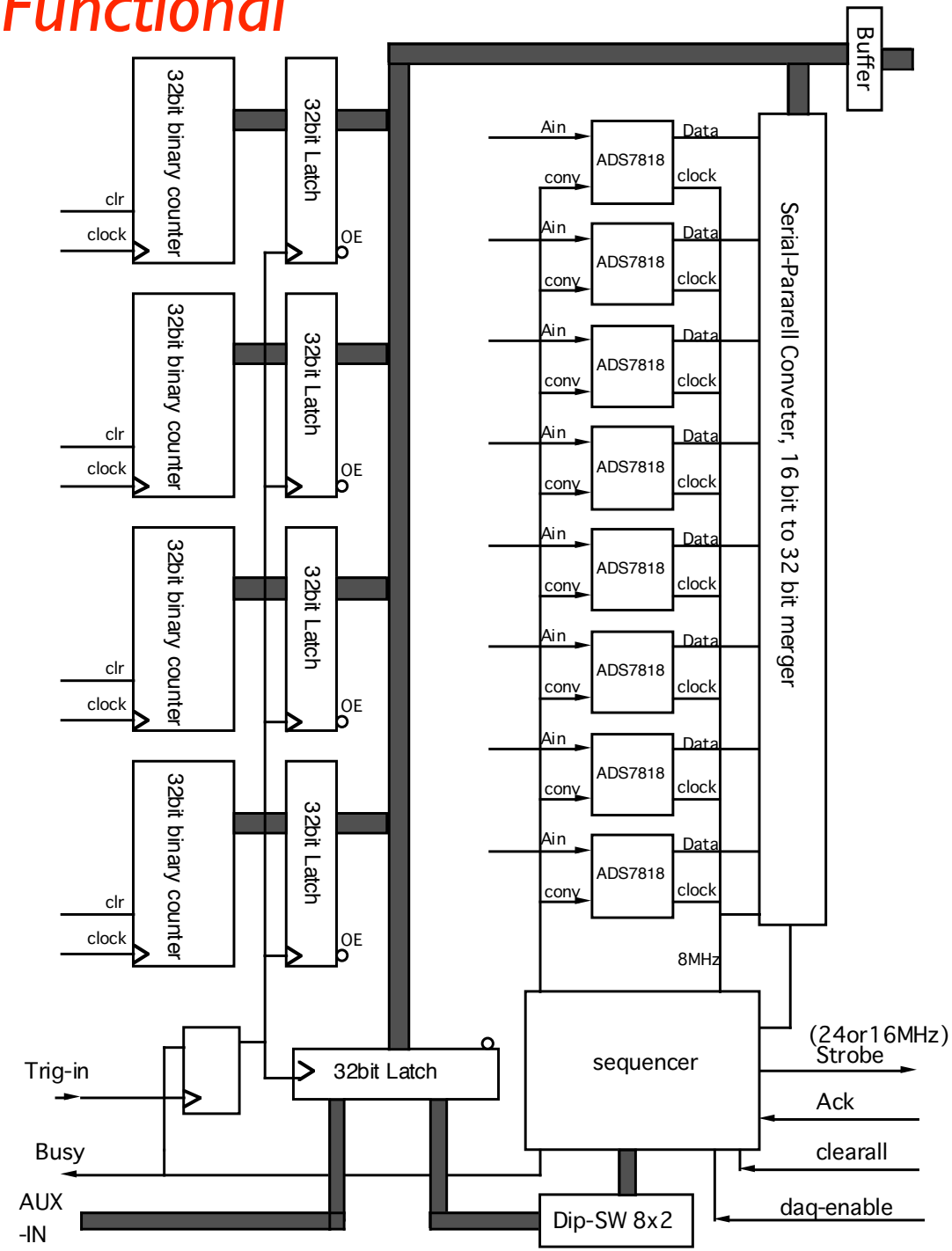
FPGA+
8 ADCs

**ADlink PCI7300A**

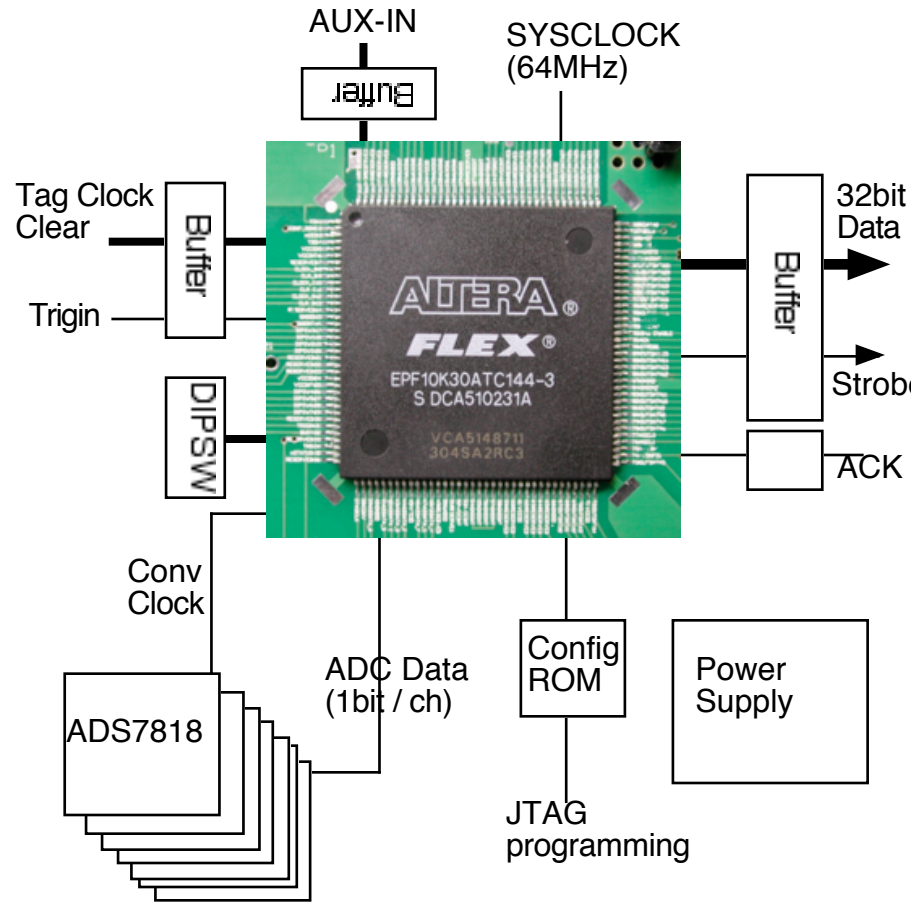
Top Performance with
Minimum Time, Skill, Cost,...

# Block Diagram of the Front-End

## *Functional*

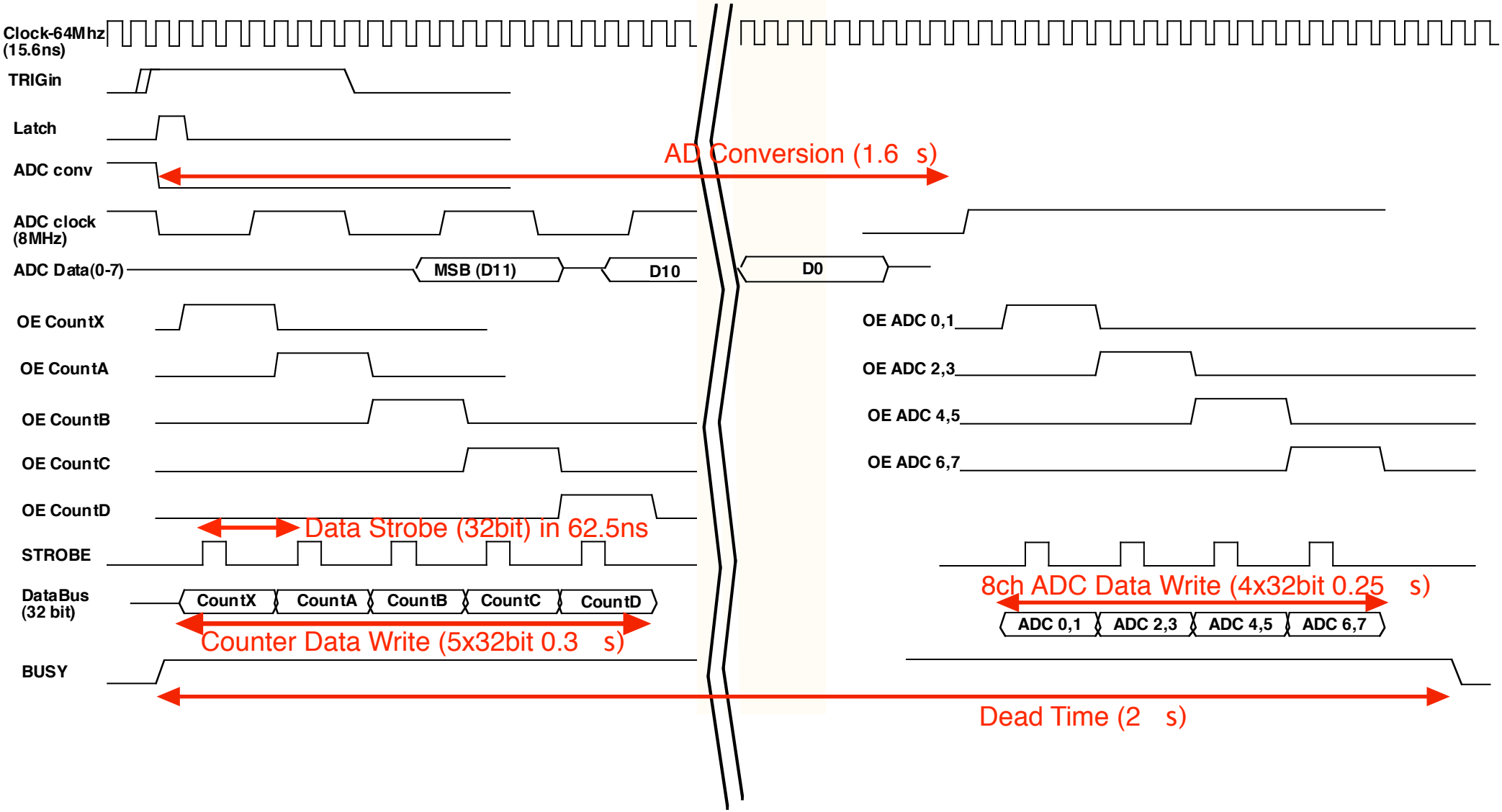



## *Geometrical*



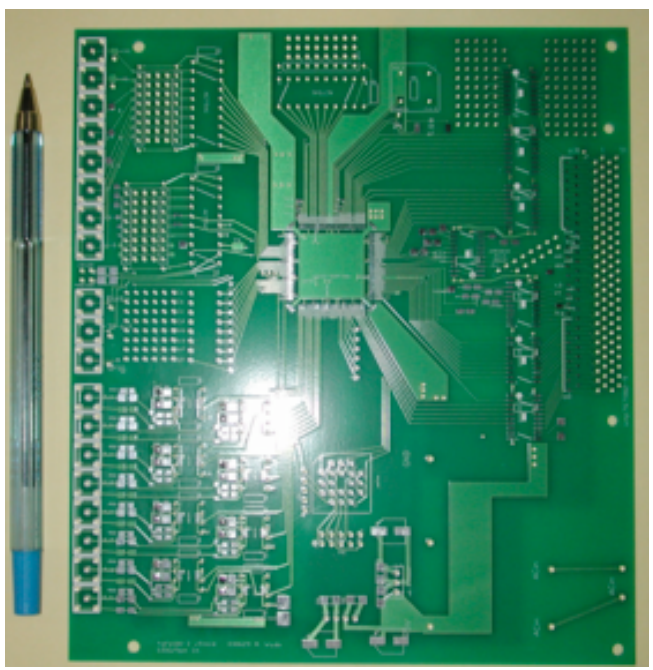

*Simply connects all signals to an FPGA.*
*HDL configures all functions in the fly.*

# Timing Chart

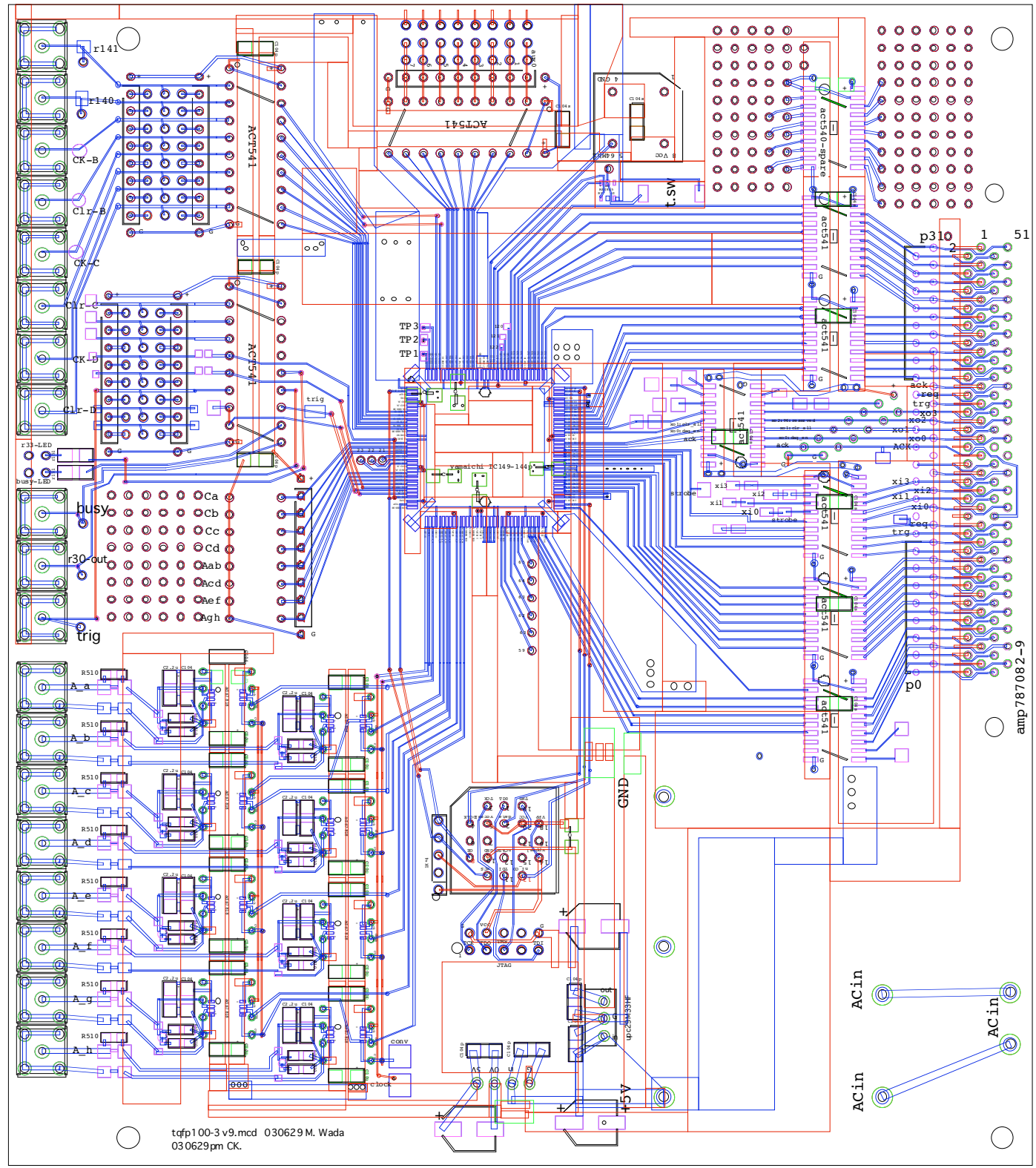


# PCB Design

*Hand wiring by mechanical CAD.*
*Convert to Gerber data.*
*VectorWorks &*
*Link CAD*



Delivery : 5 days
Cost: 50 k yen



# Programming FPGA

- HDL (hardware description language) programming

  **Verilog HDL, VHDL, SystemC, LabView-FPGA, ...**

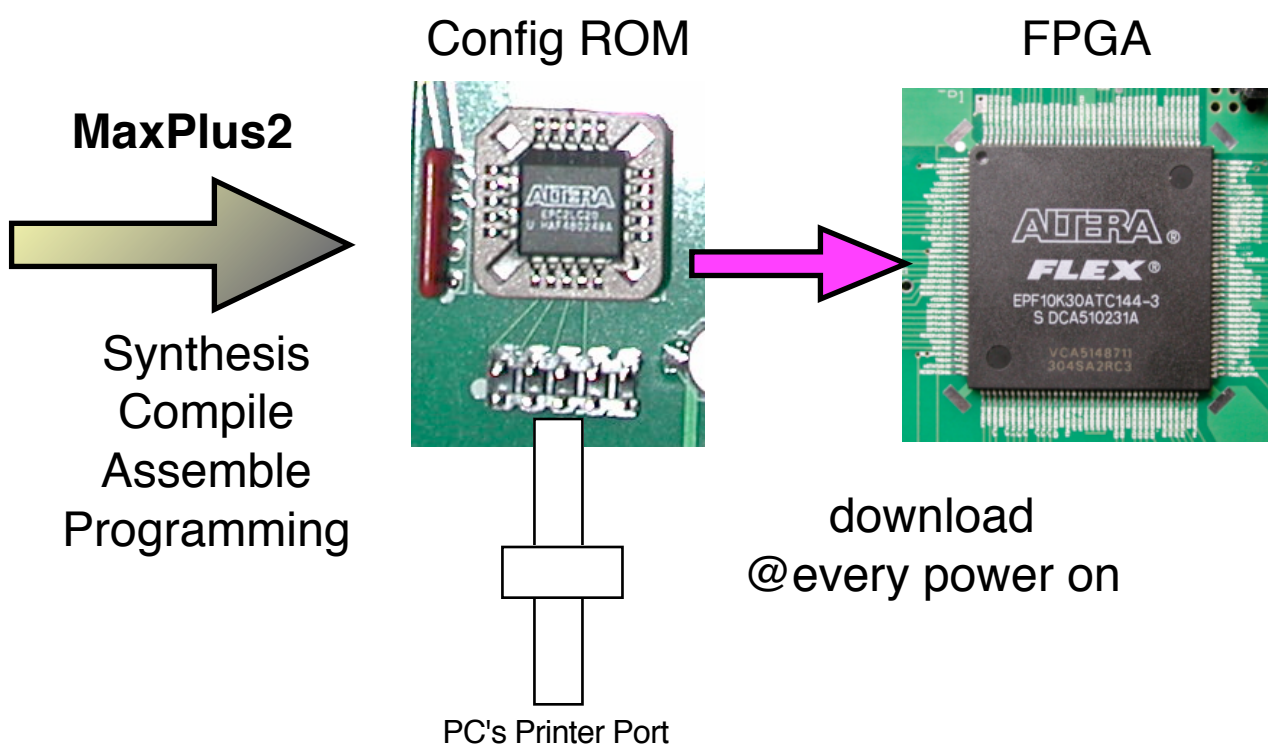
- Synthesis, Compile, Assemble, Programming

  **MaxPlus 2 Base-line + MaxPlus2 Advanced** by ALTERA (for free)

*example of Verilog HDL code*

```
// counter X (16bit Event Counter)
always @ ( posedge TRIG ) begin
      if ( DAQE == 0 )
            COUNTXO <= 16'h0;
      else
            COUNTXO <= COUNTXO + 16'h1;
end

// counter A  CLK1MHz COUNT
always @ ( posedge CLK1MHZ ) begin
      if ( DAQE == 0 )
            COUNTAO <= 32'h0;
      else
            COUNTAO <= COUNTAO + 32'h1;
end
```



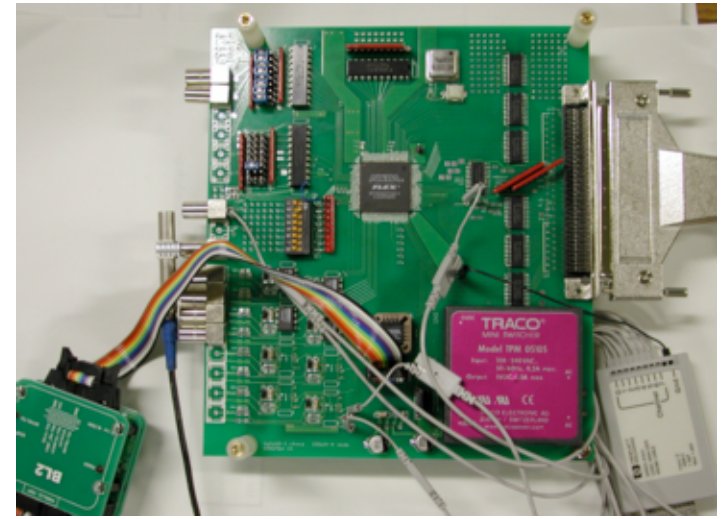
# Field Test

- PCB Debug

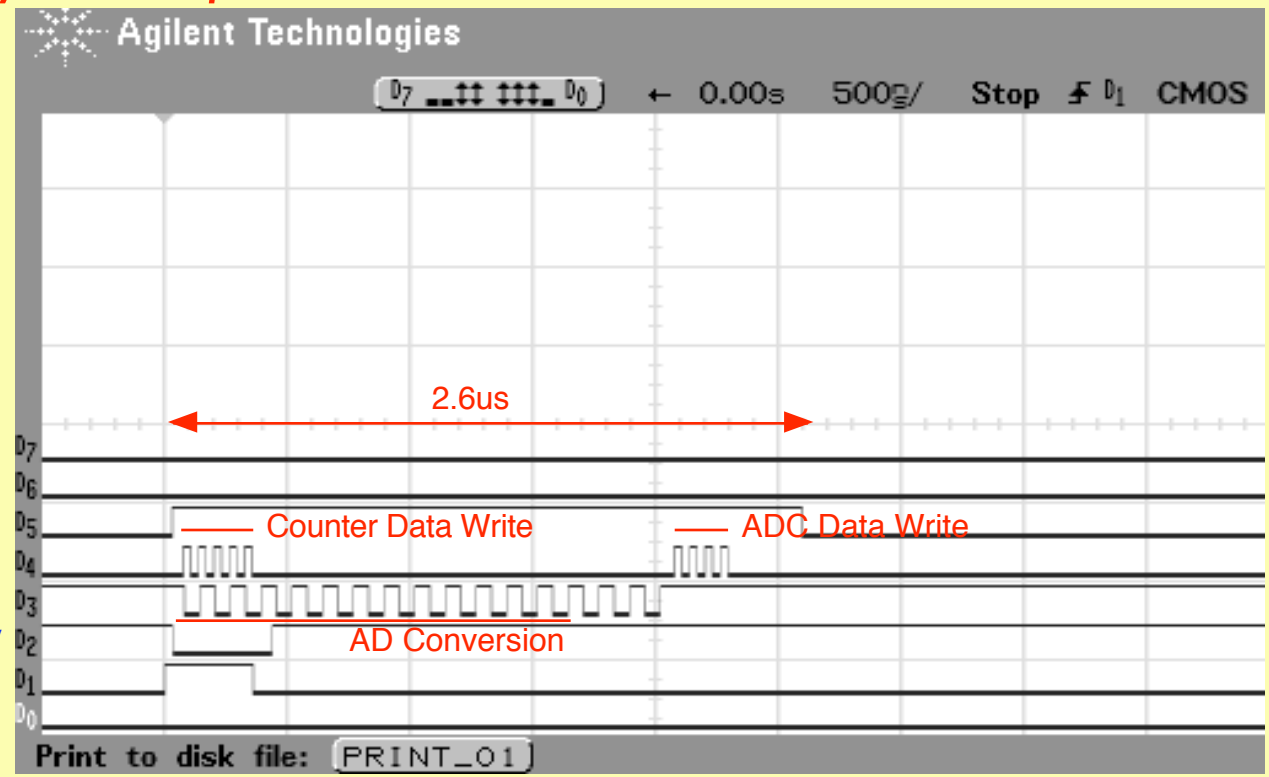
  some miss connections found.
  fixed by jumper cables

- FPGA Debug

  some data are incorrect.
  Verilog HDL program modification fixes.



*Logic Analyzer Output*



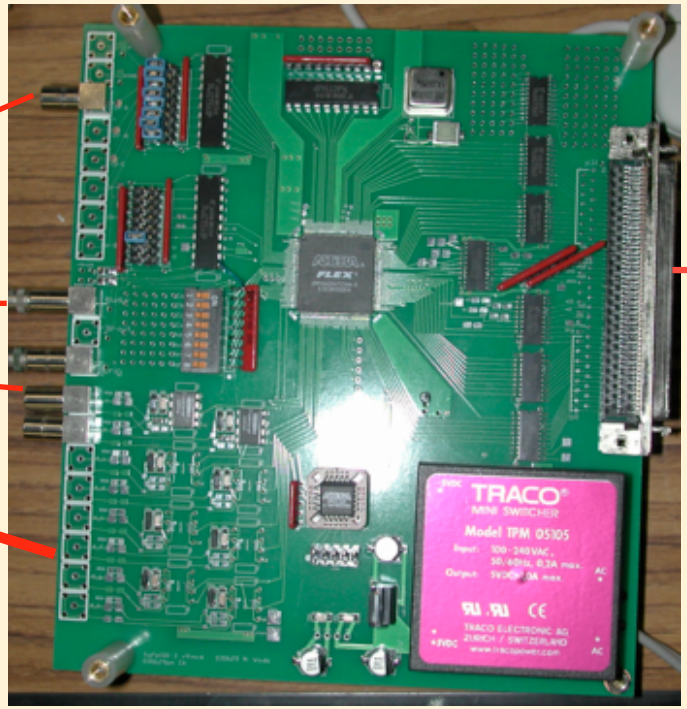
# Back End

RealTime Linux
(RTAI)

```
acquisition()
{
// initializations
while(1){
        rt_sem_wait(&10msec_timer);
        Read_FIFO_port_until_empty(buf);
        Write_rtFIFO(buf);
}
```

32bit DIO
with FIFO

ADLink PCI7300A




a PCB with an FPGA
and 8 ADC

**PC**

**PC**

GUI
LabView

# Summary

- Simple, Fast DAQ Front-end was build

  with Minimum Effort

- Extensions

  **More ADC's**

- **1pin/ch, 62.5 ns/2ch DT increase**

  **Precision ADC, TDC inputs**

  **buy converter modules from Philips?**

- **Paralell DAQ (Many independent Fron-ends)**

  **Synchronization with EventCountTag**

  **+ RF frequency Count Tag**

- **More Advanced DAQ**

  **DSP+FPGA System**

- Don't hesitate to build own hardwares for particular experiments