LHC-ATLAS実験の トリガーシステム

坂本　宏

東京大学素粒子物理

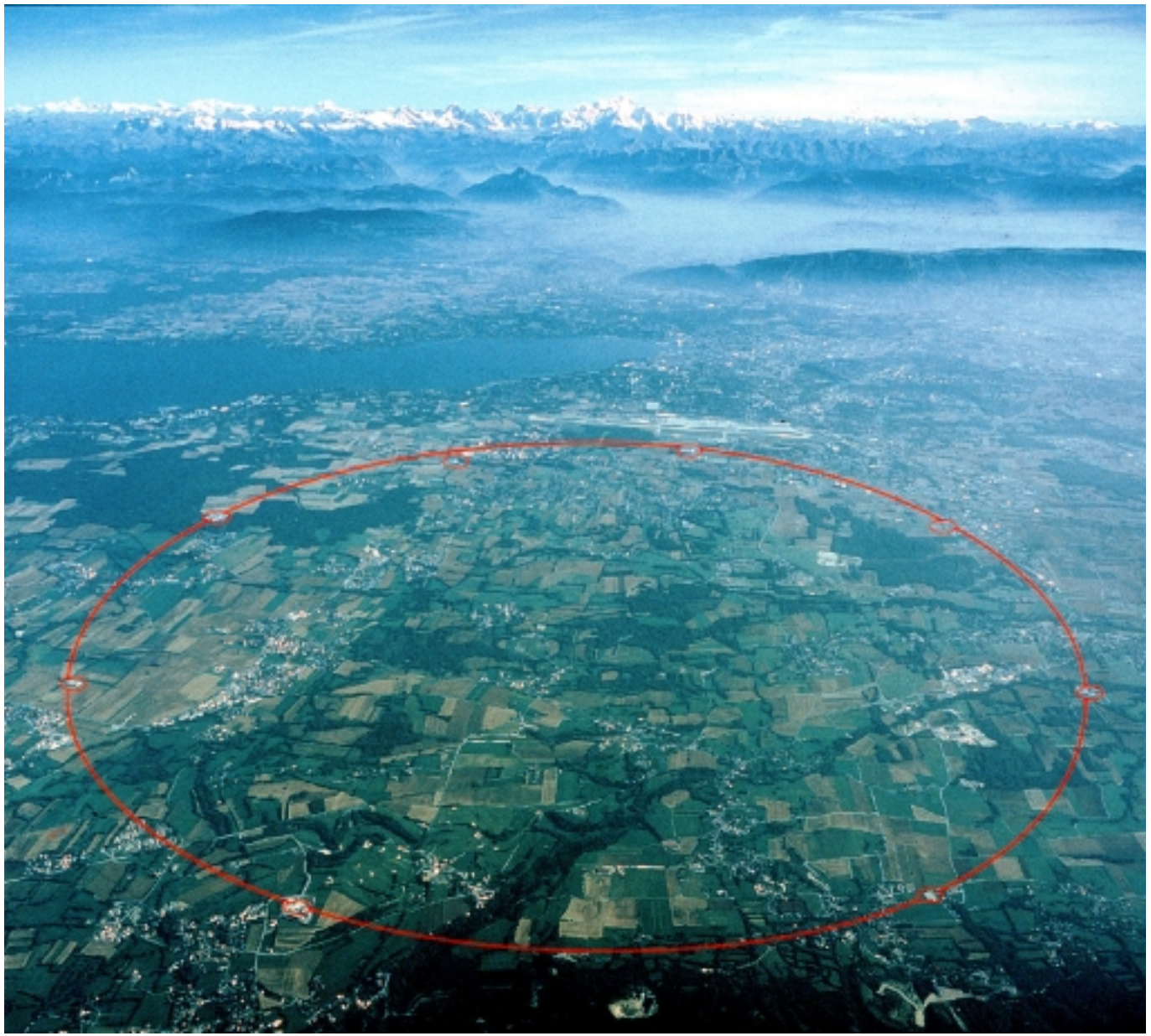
国際研究センター

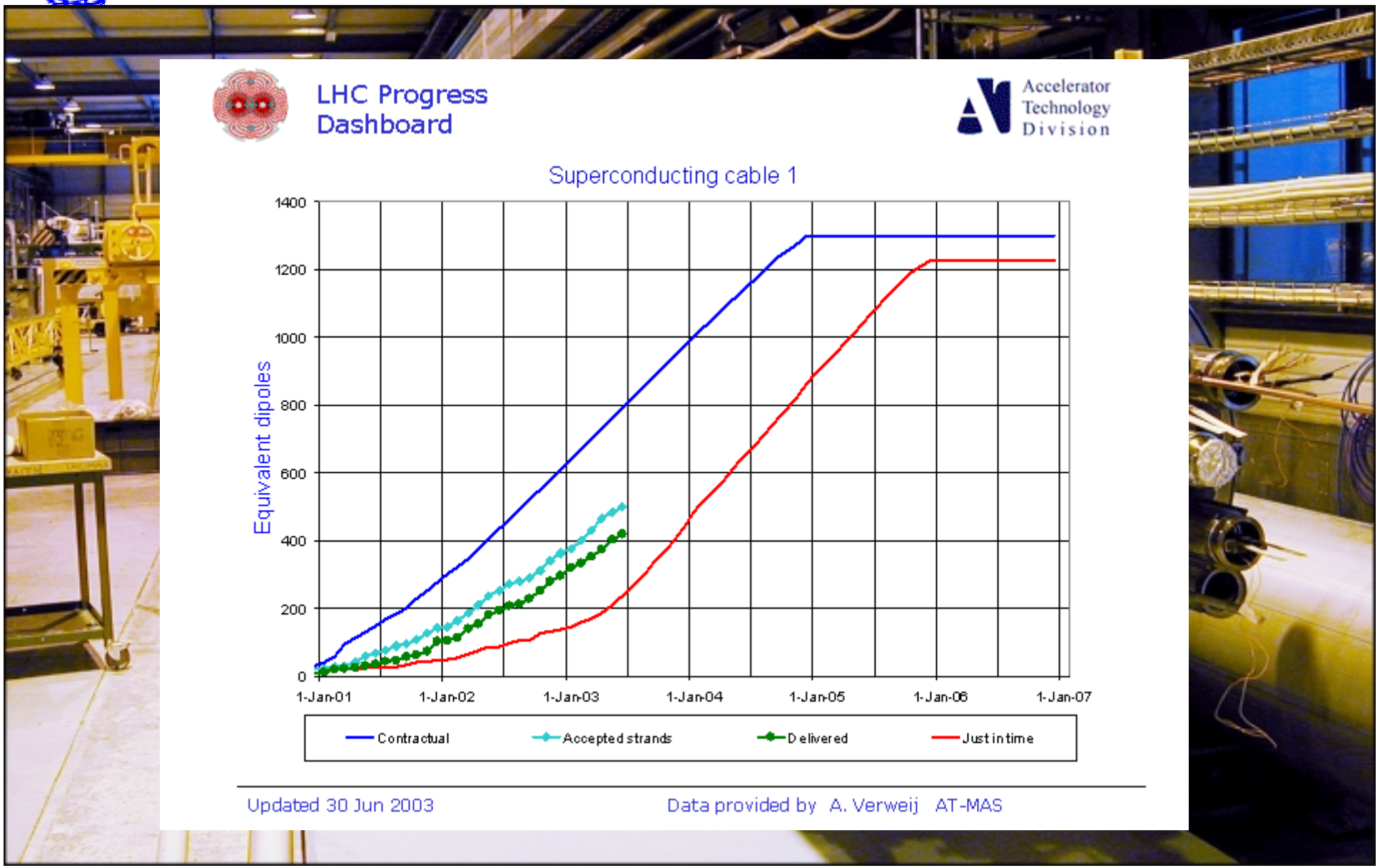
内容

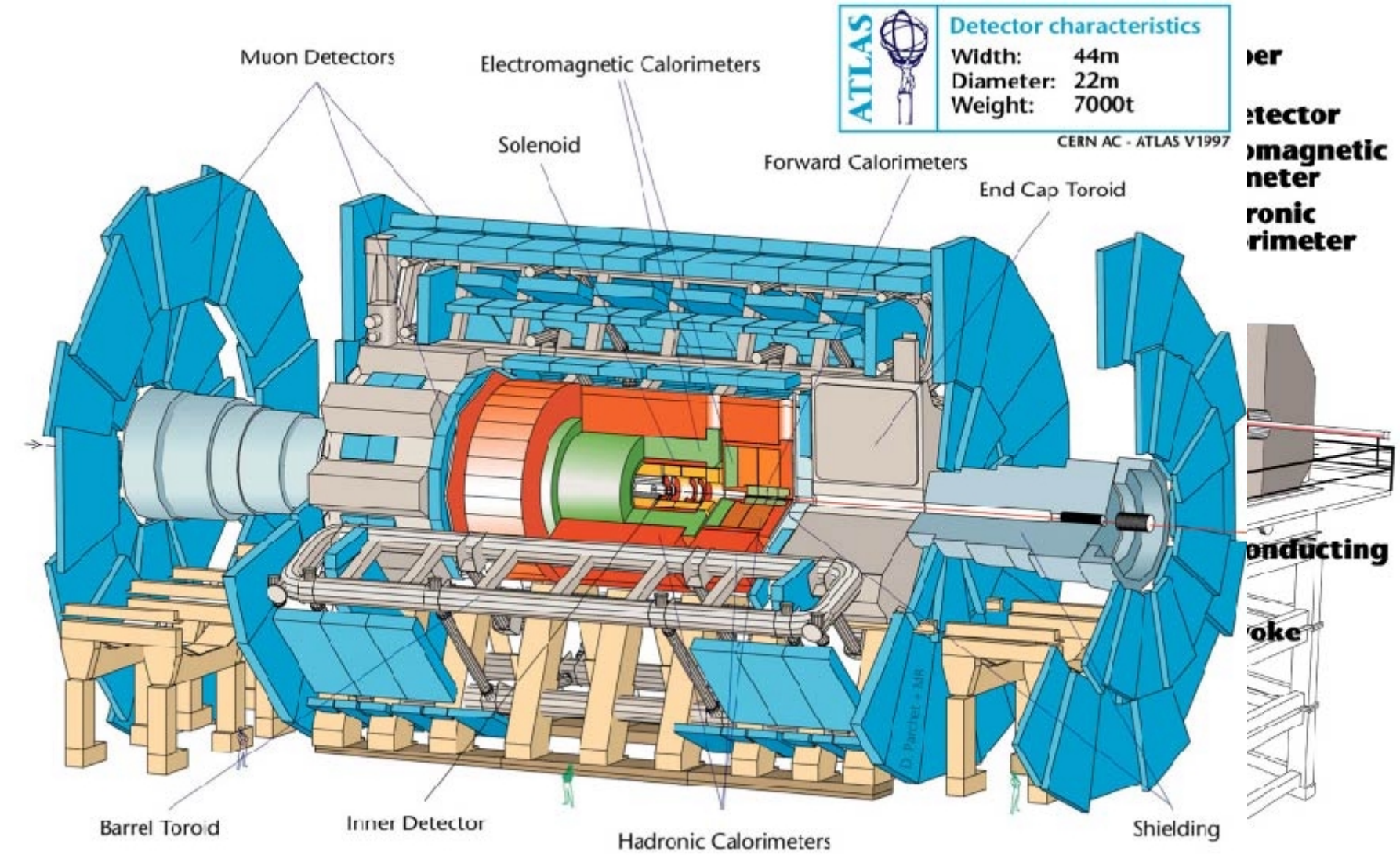
- ATLAS実験の概要
- ATLAS実験のトリガー・DAQへの要請
- トリガー戦略
- レベル1トリガーの実際
  - 概要
  - ミューオントリガーの実装
- 高位トリガーの実際

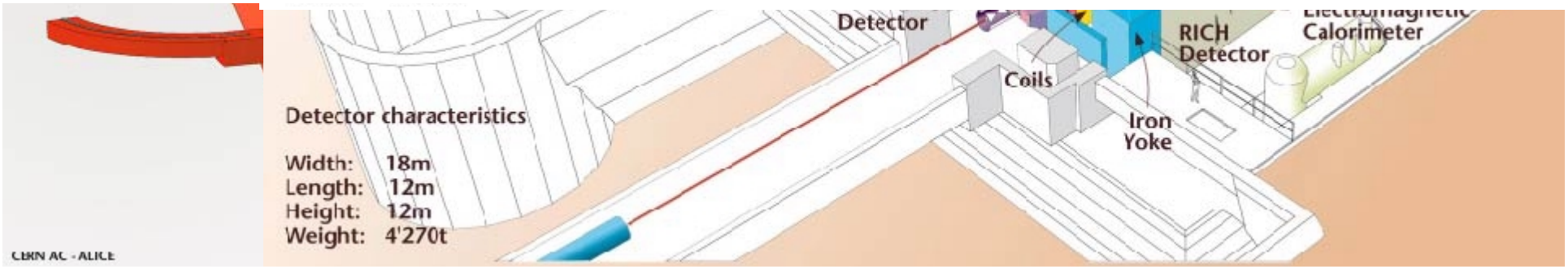
LHC-ATLAS実験

- LHC加速器
  - 7TeV+7TeV陽子・陽子衝突器
  - $L=1\times10^{34}cm^{-2}s^{-1}$
  - バンチ交叉40MHz=バンチ間隔25ns
  - ミニマムバイアス100mb=1GHzイベントレート



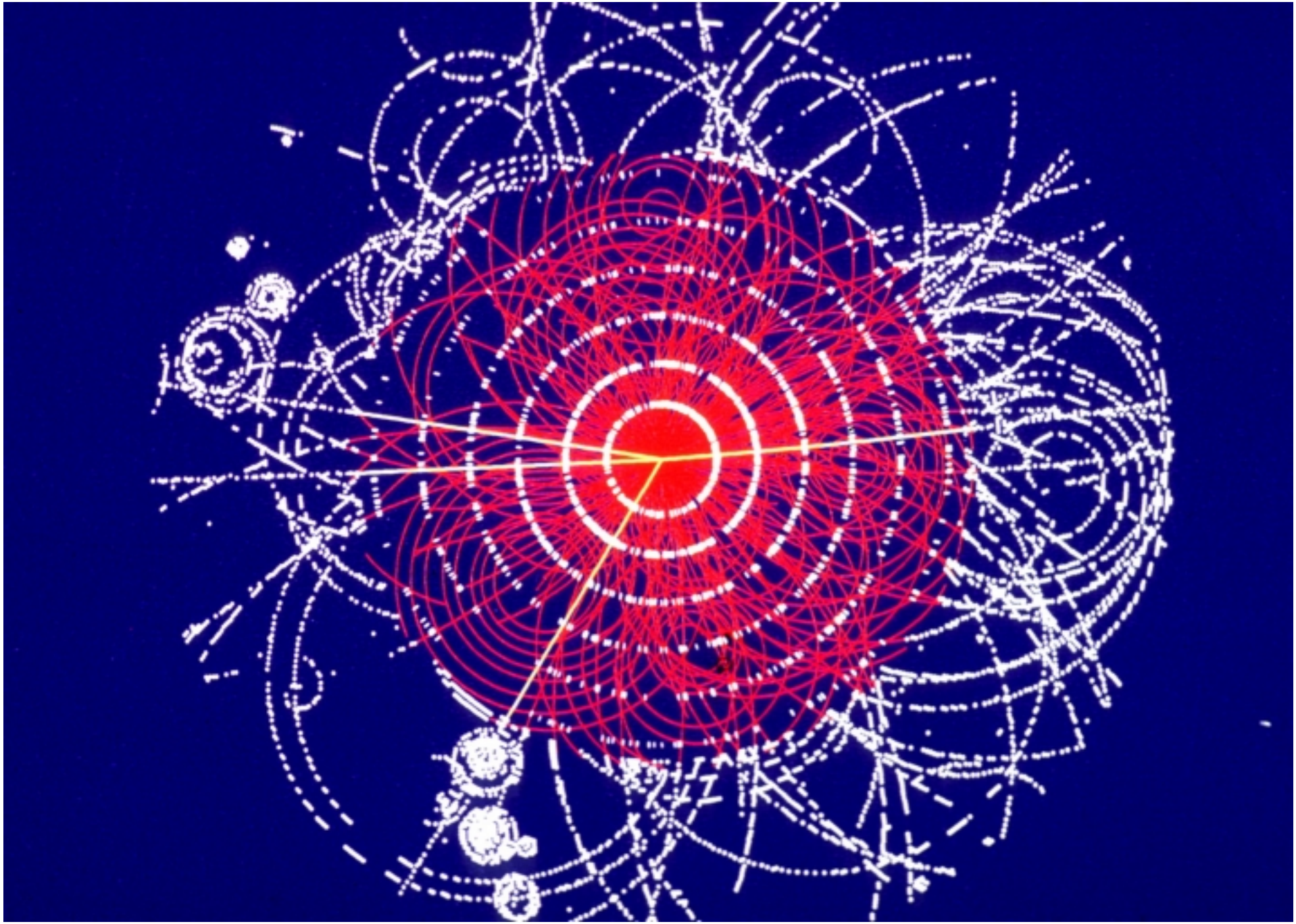

LHC Progress Dashboard
Accelerator Technology Division
Superconducting cable 1
Equivalent dipoles
1400
1200
1000
800
600
400
200
0
1-Jan-01
1-Jan-02
1-Jan-03
1-Jan-04
1-Jan-05
1-Jan-06
1-Jan-07
Contractual
Accepted strands
Delivered
Just in time
Updated 30 Jun 2003
Data provided by A. Verweij AT-MAS

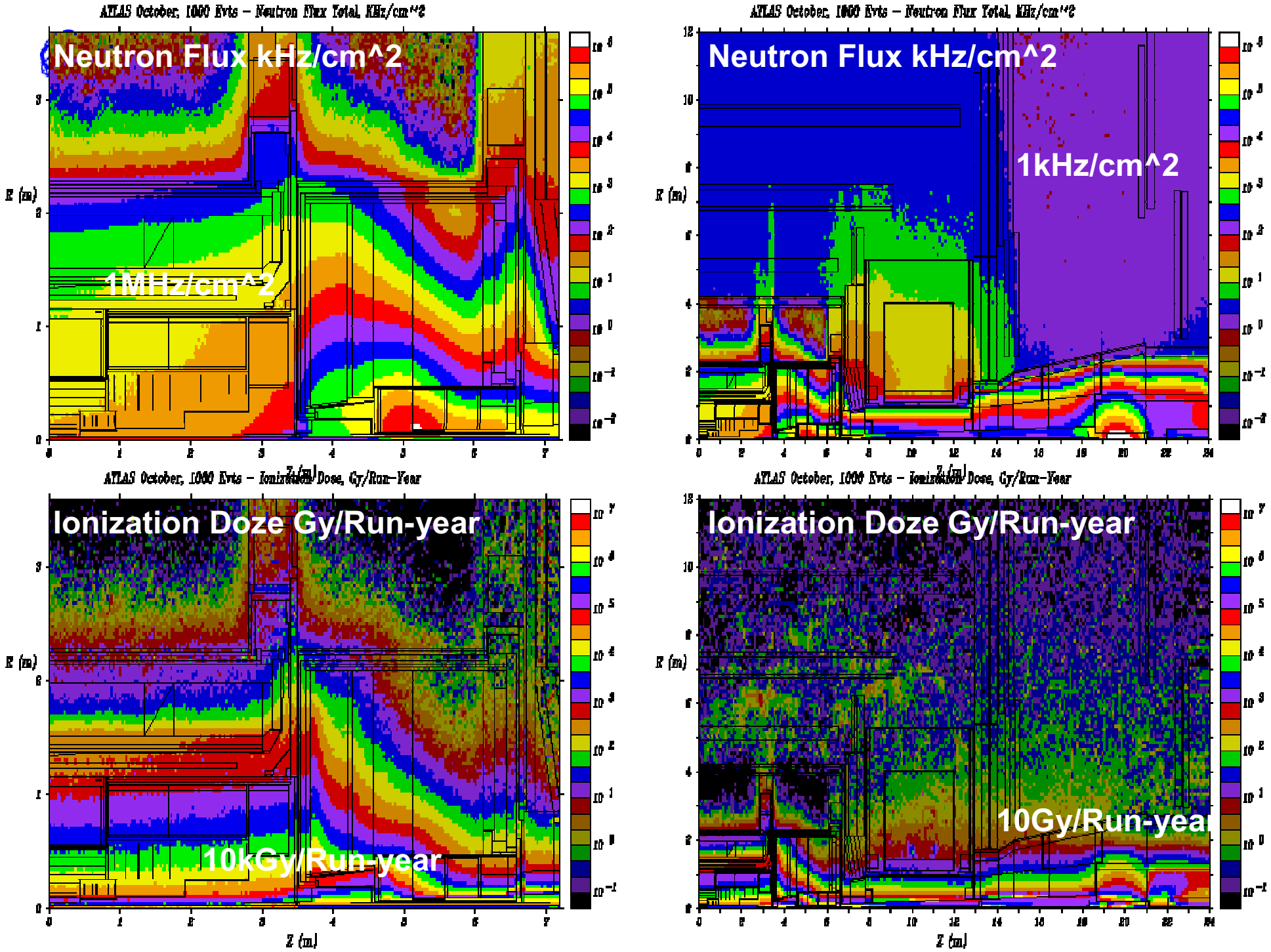

ATLAS
Detector characteristics
Width: 44m
Diameter: 22m
Weight: 7000t
CERN AC - ATLAS V1997
Muon Detectors
Electromagnetic Calorimeters
Solenoid
Forward Calorimeters
End Cap Toroid
Barrel Toroid
Inner Detector
Hadronic Calorimeters
Shielding

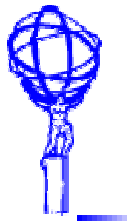

Detector
RICH Detector
Calorimeter
Coils
Iron Yoke
Detector characteristics
Width: 18m
Length: 12m
Height: 12m
Weight: 4'270t
CERN AC - ALICE

トリガー・DAQへの要請

- データサイズ
  - 1億チャンネル強の読み出し
  - イベントあたり2MB
- トリガーレート
  - ミニマムバイアス1GHz
  - 物理トリガー140Hz
- 放射線環境
  - 10年で10krad~1Mrad
    - TID (Total Ionization Doze)
    - SEE (Single Event Effect)

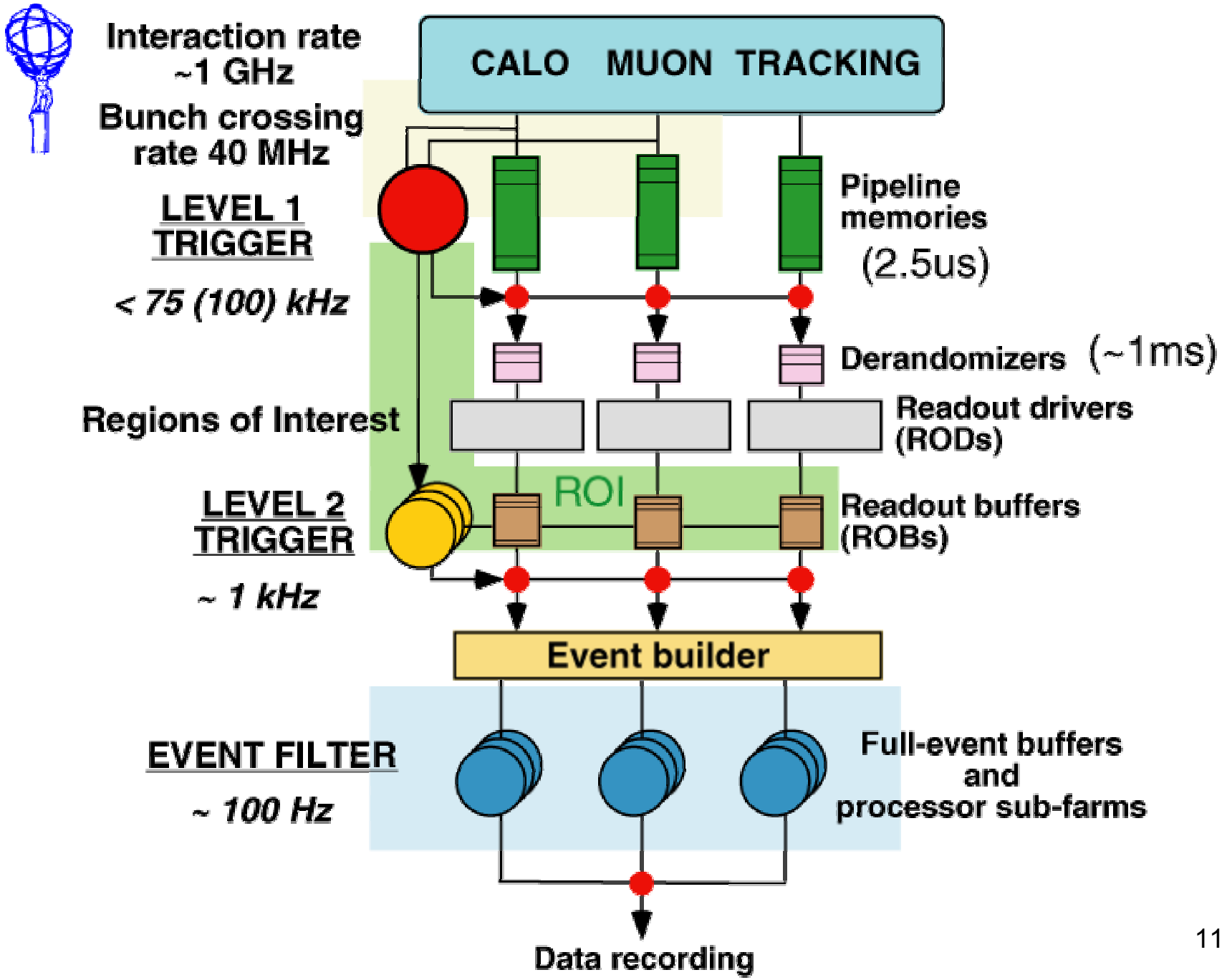



ATLAS October, 1000 Evts – Neutron Flux Total, kHz/cm**2
Neutron Flux kHz/cm^2
1MHz/cm^2
R (m)
Z (m)
ATLAS October, 1000 Evts – Neutron Flux Total, kHz/cm**2
Neutron Flux kHz/cm^2
1kHz/cm^2
R (m)
Z (m)
ATLAS October, 1000 Evts – Ionisation Dose, Gy/Run-Year
Ionization Doze Gy/Run-year
10kGy/Run-year
R (m)
Z (m)
ATLAS October, 1000 Evts – Ionisation Dose, Gy/Run-Year
Ionization Doze Gy/Run-year
10Gy/Run-year
R (m)
Z (m)



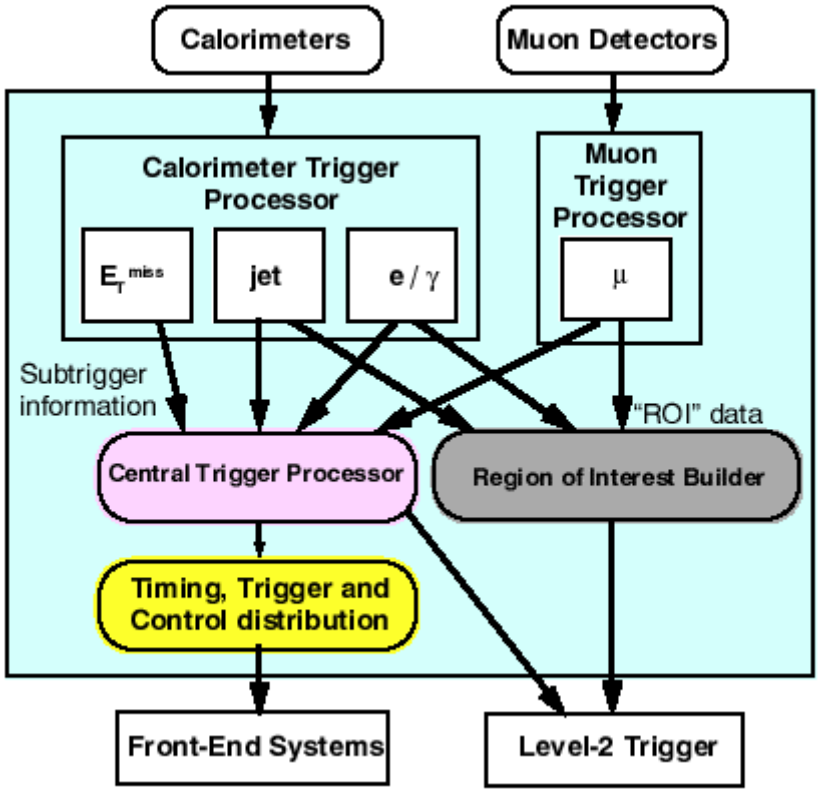
トリガー戦略

- 多段トリガーの採用
  - レベル1
    - パイプライン、専用ハード、2μs
    - カロリメータとミューオンのみ
  - レベル2
    - バッファメモリ、PCファーム、10ms
    - 検出器の全分解能だがRoIのみ
  - イベントビルダー
  - レベル3
    - イベントフィルター、PCファーム
    - 全データの利用


Interaction rate
~1 GHz
Bunch crossing
rate 40 MHz
LEVEL 1
TRIGGER
< 75 (100) kHz
CALO MUON TRACKING
Pipeline
memories
(2.5us)
Derandomizers (~1ms)
Readout drivers
(RODs)
Regions of Interest
ROI
LEVEL 2
TRIGGER
~ 1 kHz
Readout buffers
(ROBs)
Event builder
EVENT FILTER
~ 100 Hz
Full-event buffers
and
processor sub-farms
Data recording

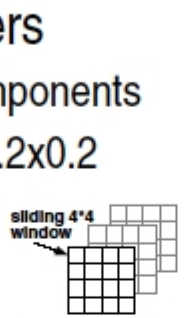
レベル1トリガーの実際

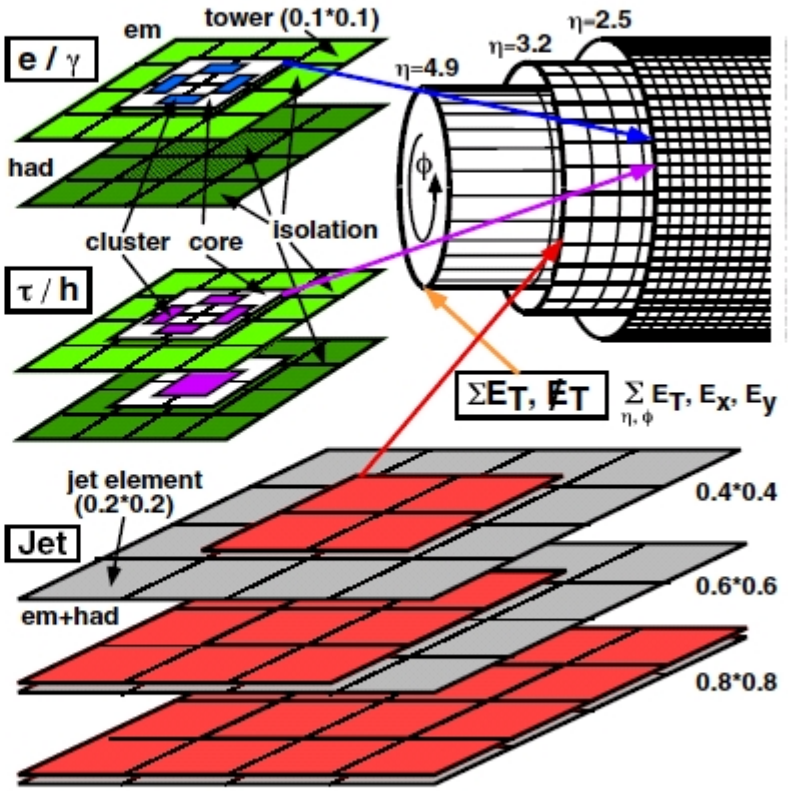
- レベル1への入力
  - カロリメータ
  - ミューオンシステム
- トリガー判定
  - サブデテクタトリガー
  - セントラルトリガープロセッサ
- トリガー信号の配布
  - TTC (Trigger/Timing Controller)



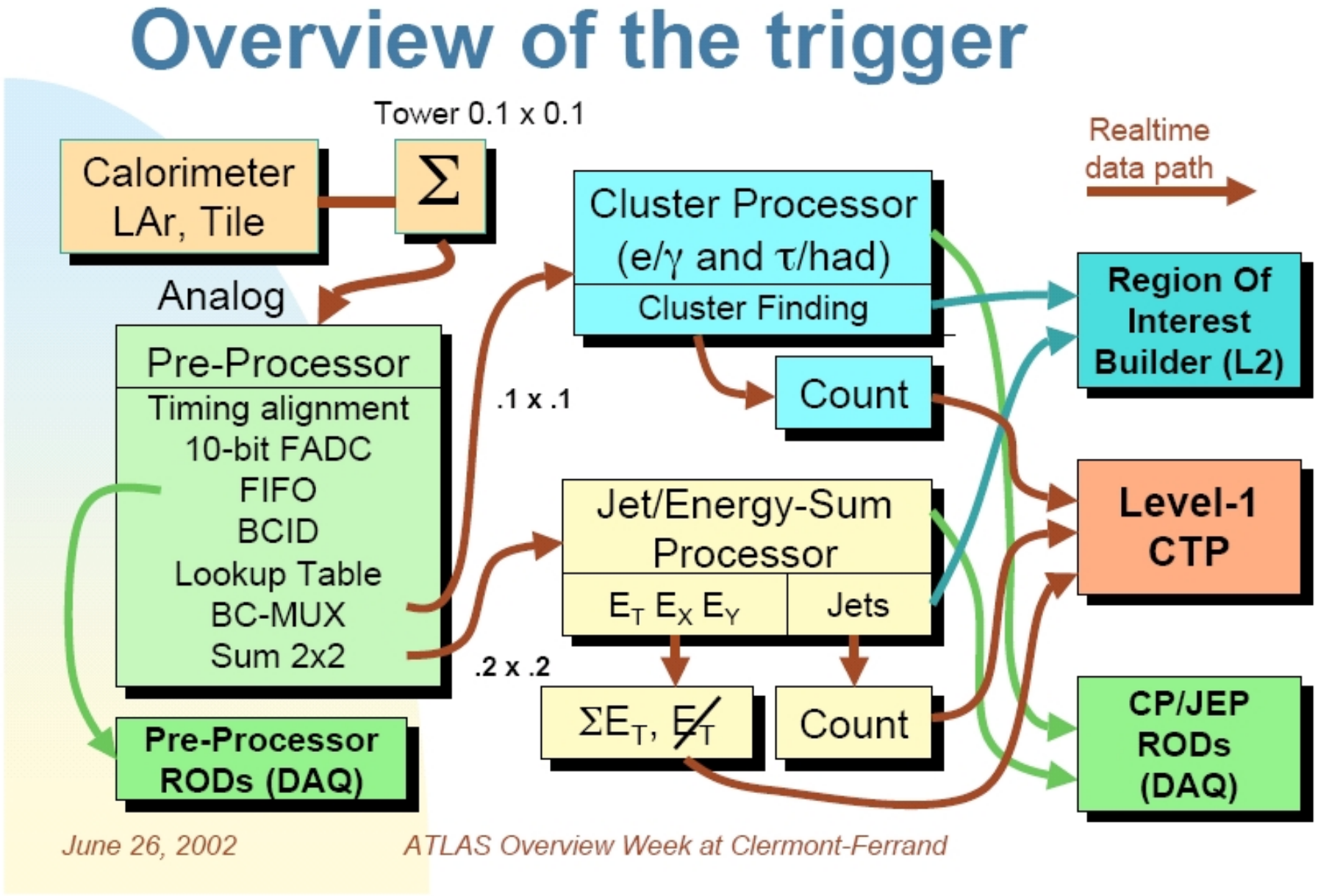
Calorimeter Trigger Algorithms I

- Analogue trigger towers
  - Separate em/had components
  - $\Delta\phi x\Delta\eta$=0.1x0.1 or 0.2x0.2
- e/γ and τ/h clusters
  - Sliding windows
  - Isolation vetoes on em and had
- Jet clusters
  - Programmable cluster size
- Energy sums
  - ΣE_T, E_t^{miss} out to $|\eta|$<4.9
- Discriminate at 8 E_T thresholds
- Cluster/jet multiplicity to CTP



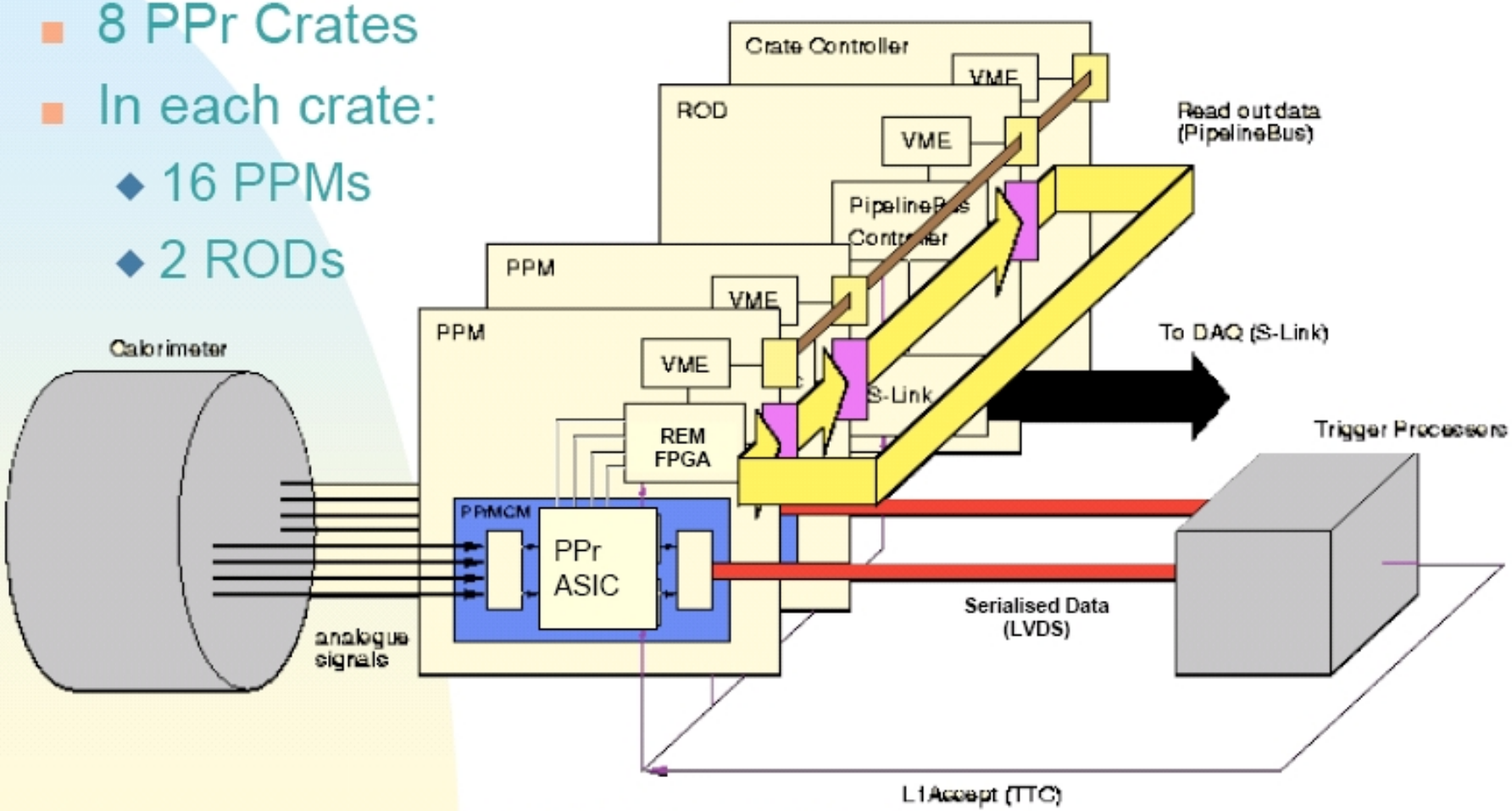


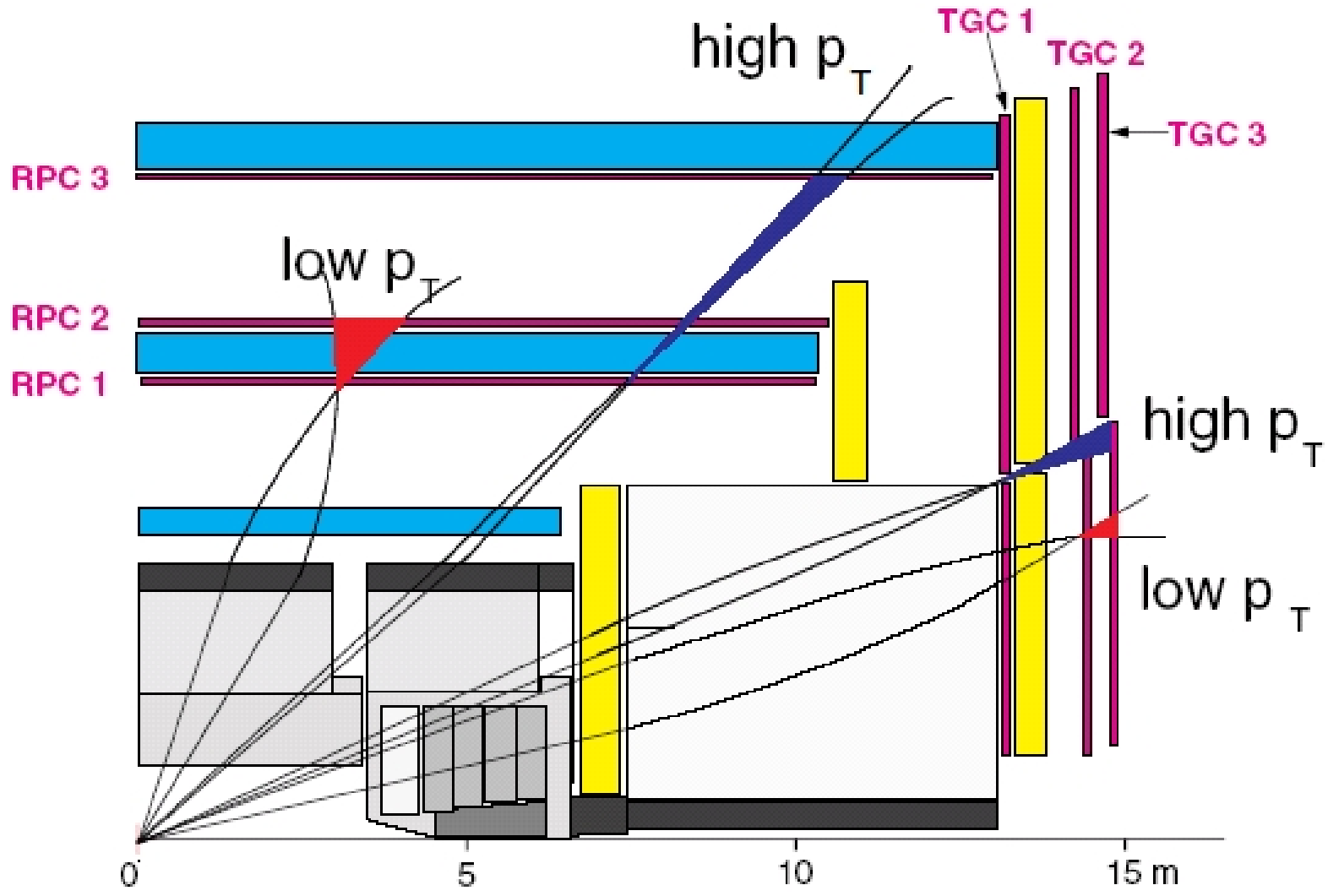
カロリメータトリガー


Overview of the trigger
Tower 0.1 x 0.1
Calorimeter
LAr, Tile
Σ
Analog
Pre-Processor
Timing alignment
10-bit FADC
FIFO
BCID
Lookup Table
BC-MUX
Sum 2x2
Pre-Processor
RODs (DAQ)
.1 x .1
.2 x .2
Cluster Processor
(e/γ and τ/had)
Cluster Finding
Count
Jet/Energy-Sum
Processor
E_T E_X E_Y
Jets
ΣE_T, E/_T
Count
Realtime
data path
Region Of
Interest
Builder (L2)
Level-1
CTP
CP/JEP
RODs
(DAQ)
June 26, 2002
ATLAS Overview Week at Clermont-Ferrand

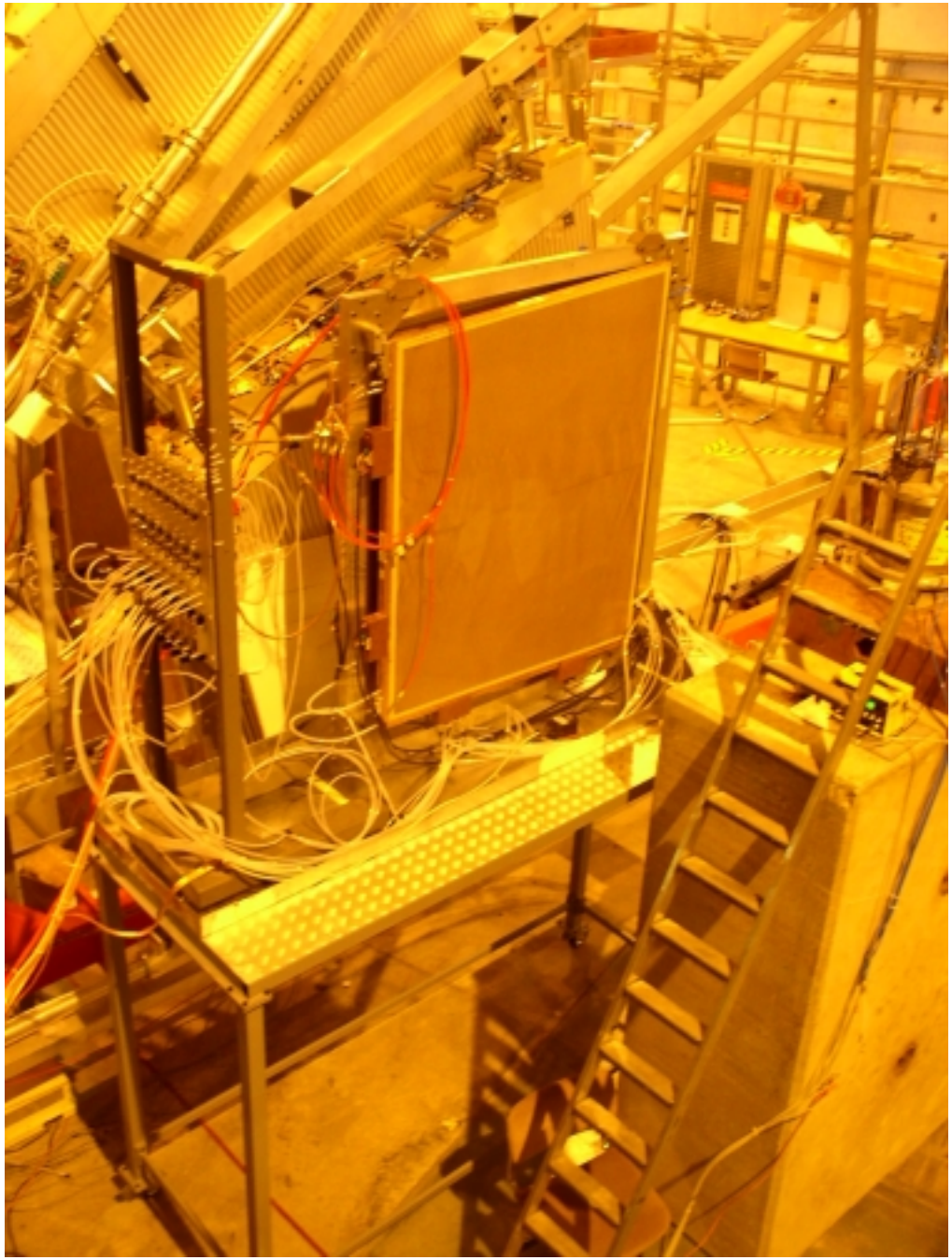
Pre-Processor sub-system

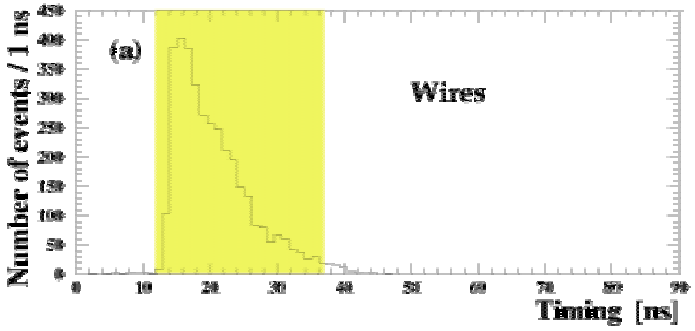
- 8 PPr Crates
- In each crate:
  - 16 PPMs
  - 2 RODs

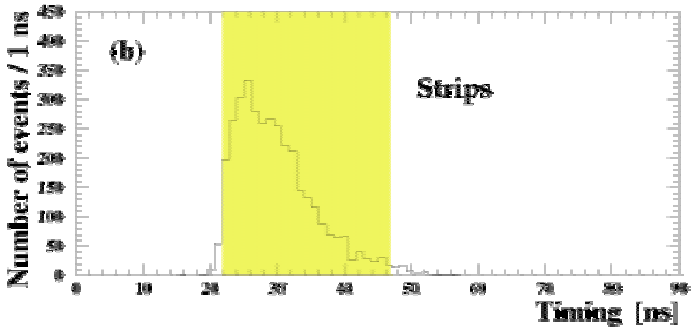


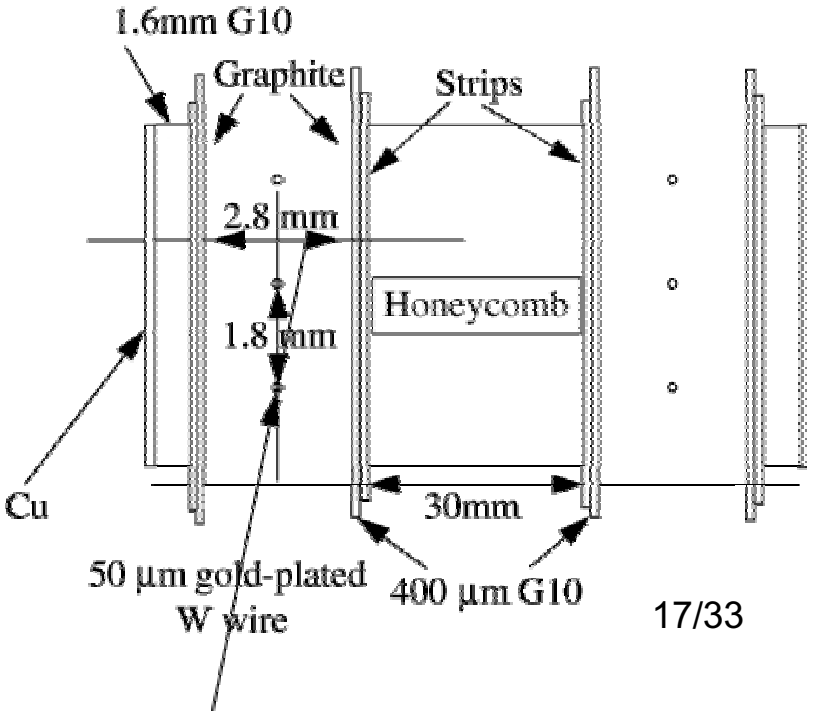


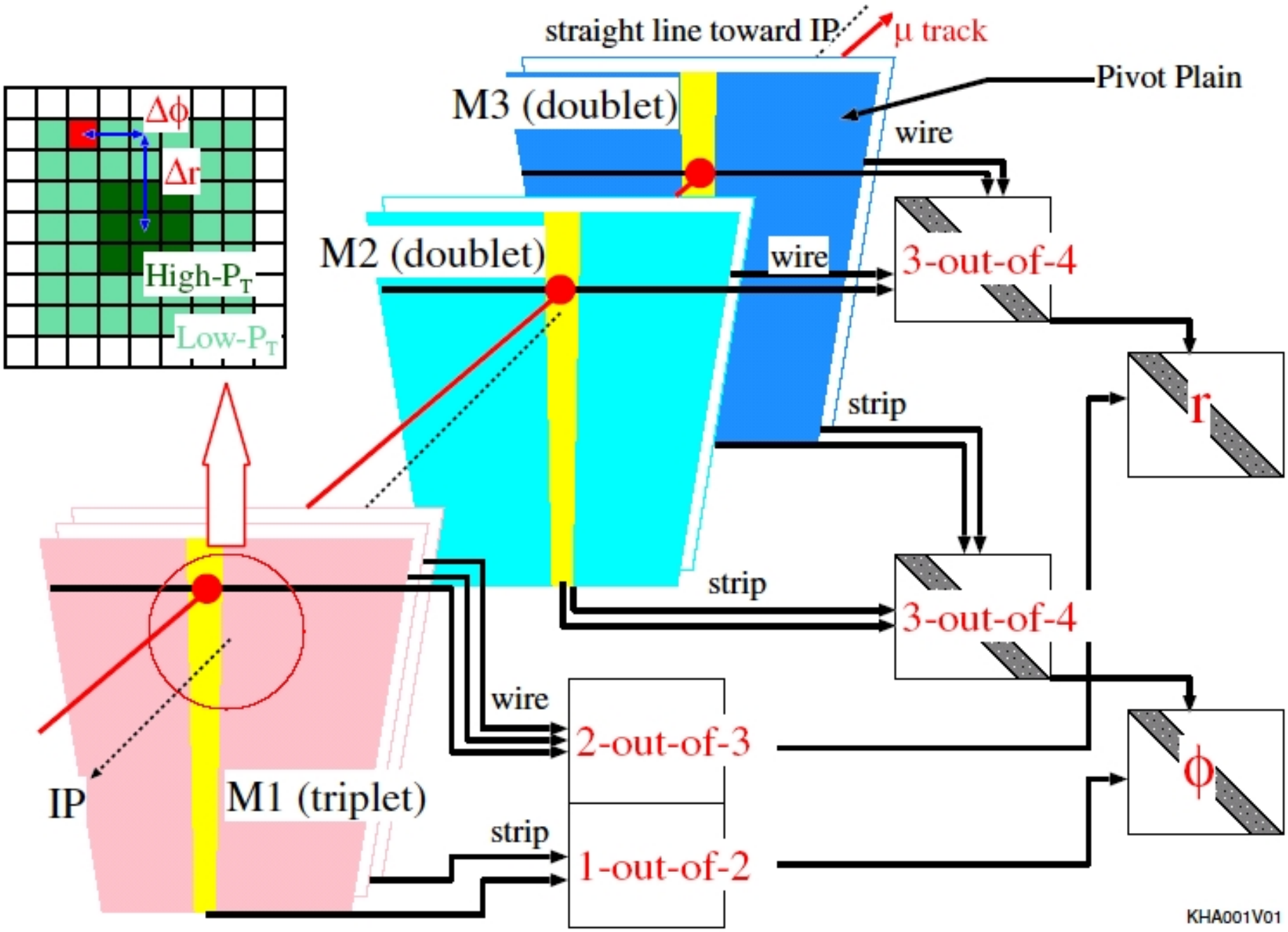
ATLAS Muon Spectrometer - Trigger scheme

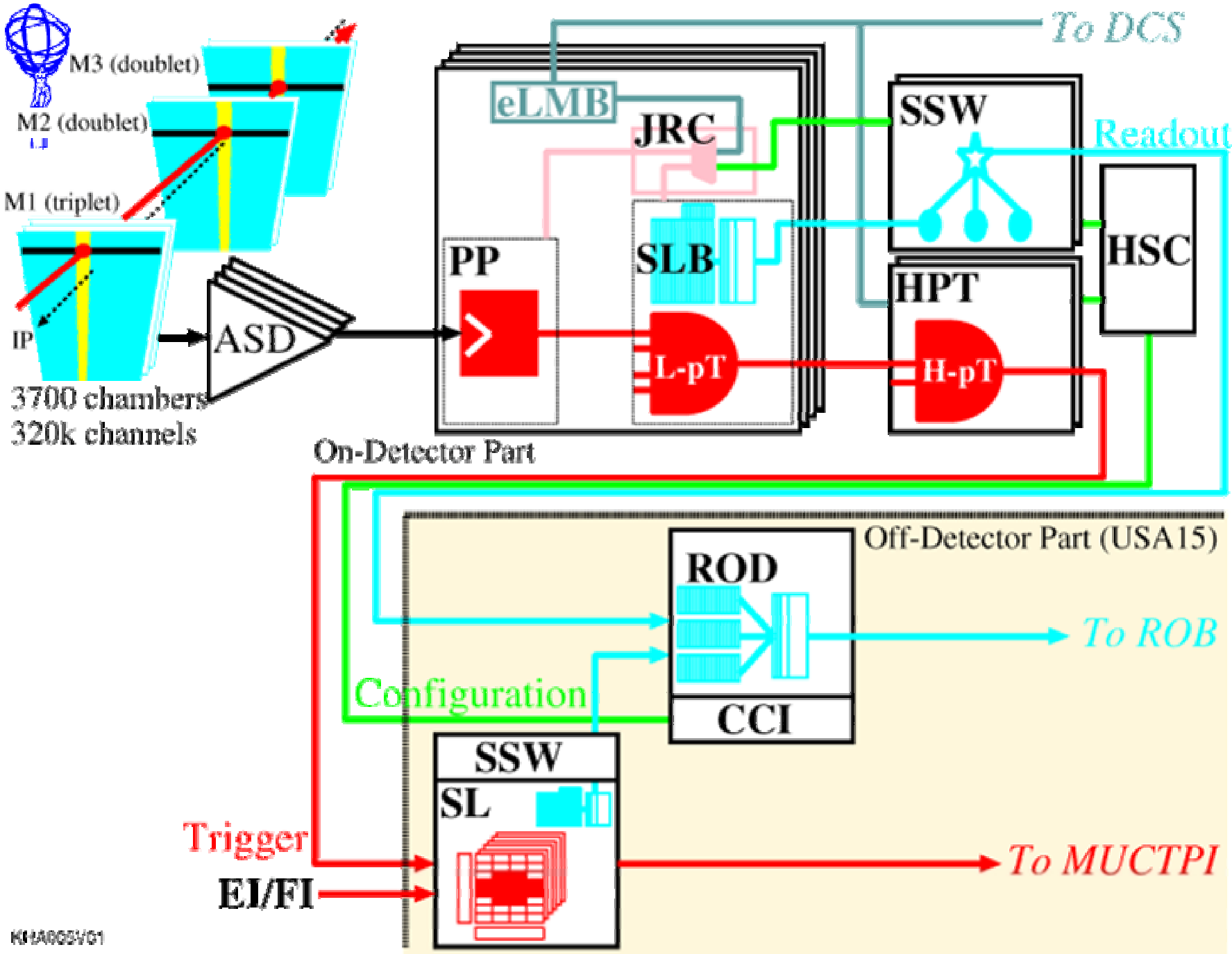


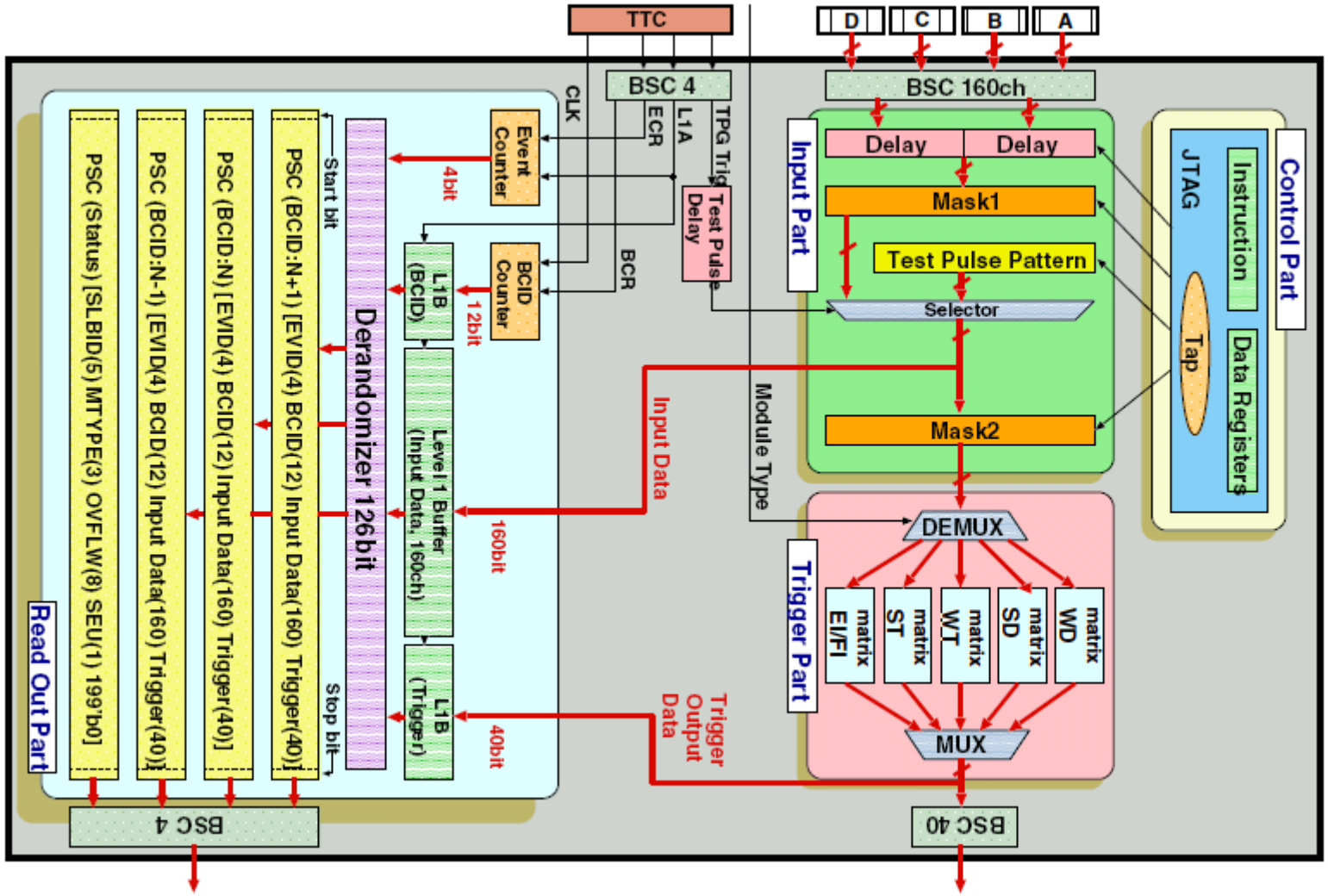

(a)
Wires
Number of events / 1 ns
Timing [ns]


(b)
Strips
Number of events / 1 ns
Timing [ns]


1.6mm G10
Graphite
Strips
2.8 mm
1.8 mm
Honeycomb
Cu
30mm
50 µm gold-plated
W wire
400 µm G10

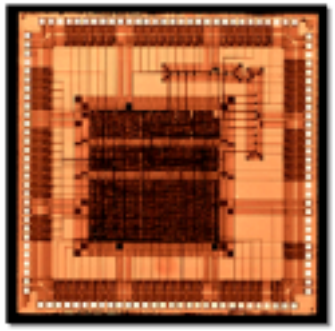

straight line toward IP
μ track
Pivot Plain
M3 (doublet)
wire
M2 (doublet)
wire
3-out-of-4
Δϕ
Δr
High-P$_T$
Low-P$_T$
r
strip
strip
3-out-of-4
wire
2-out-of-3
ϕ
IP
M1 (triplet)
strip
1-out-of-2
KHA001V01


M3 (doublet)
M2 (doublet)
M1 (triplet)
IP
ASD
3700 chambers
320k channels
To DCS
eLMB
JRC
SSW
Readout
PP
SLB
HSC
HPT
L-pT
H-pT
On-Detector Part
Off-Detector Part (USA15)
ROD
To ROB
Configuration
CCI
SSW
SL
Trigger
EI/FI
To MUCTPI


TTC
D
C
B
A
BSC 4
BSC 160ch
CLK
ECR
L1A
TPG Trig
Test Pulse Delay
BCR
Delay
Delay
Mask1
Test Pulse Pattern
Selector
Mask2
Input Part
Control Part
Instruction
Data Registers
JTAG
Tap
Module Type
Input Data
Event Counter
4bit
BCID Counter
12bit
L1B (BCID)
Level 1 Buffer (Input Data, 160ch)
160bit
L1B (Trigger)
40bit
Derandomizer 126bit
Start bit
Stop bit
Read Out Part
PSC (BCID:N+1) [EVID(4) BCID(12) Input Data(160) Trigger(40)]
PSC (BCID:N) [EVID(4) BCID(12) Input Data(160) Trigger(40)]
PSC (BCID:N-1) [EVID(4) BCID(12) Input Data(160) Trigger(40)]
PSC (Status) [SLBID(5) MTYPE(3) OVFLW(8) SEU(1) 199'b0]
BSC 4
DEMUX
matrix EI/FI
matrix ST
matrix WT
matrix SD
matrix WD
MUX
Trigger Part
Trigger Output Data
BSC 40

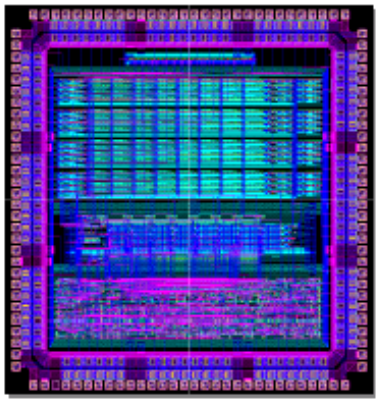
トリガー用ASIC

ROHM 0.6μm
4.5x4.5mm^2



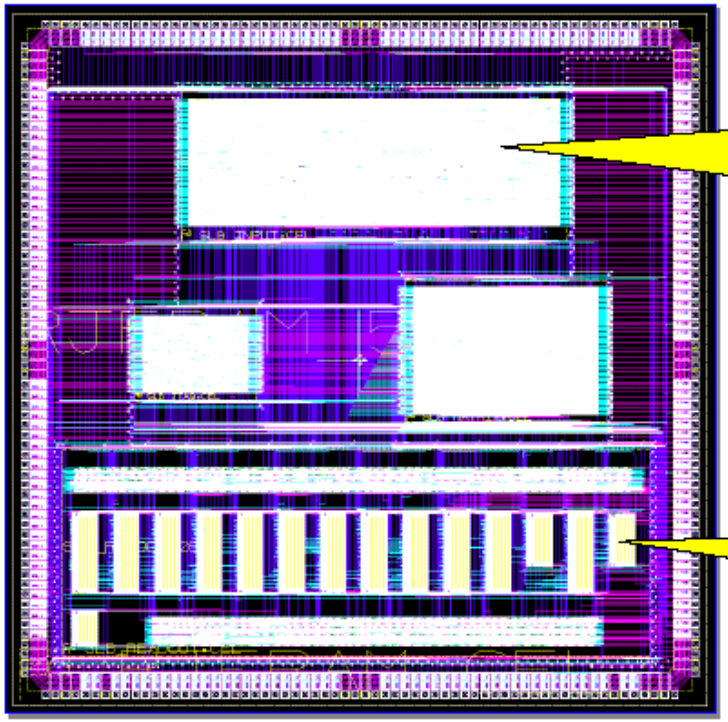
MWPC-readout
final version
(rad test)

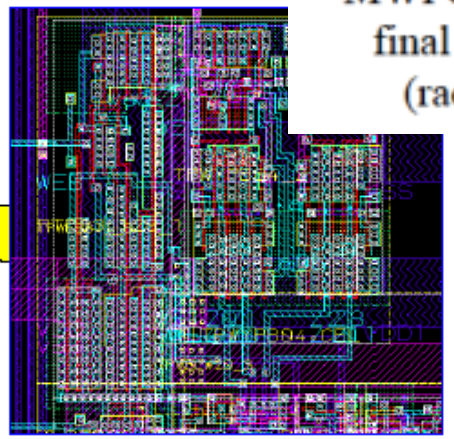
ROHM 0.6μm
4.5x4.5mm^2



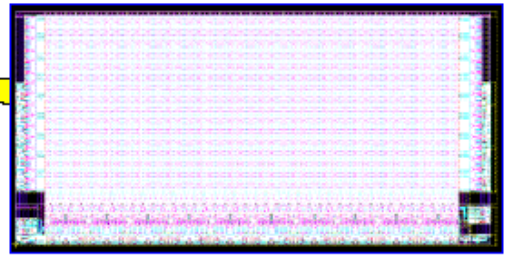
PP-ASIC
integrated 16ch

Full spec. SLB ASIC
(ROHM 0.35μm**) 9.7x9.7mm^2**



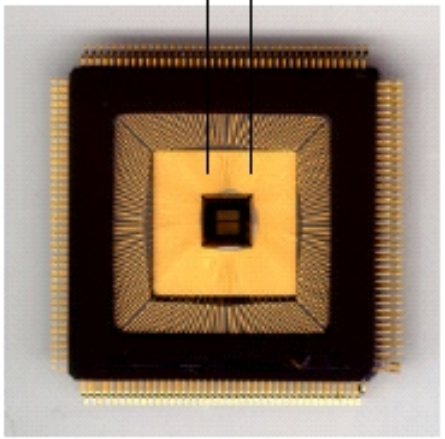


Enlarged view

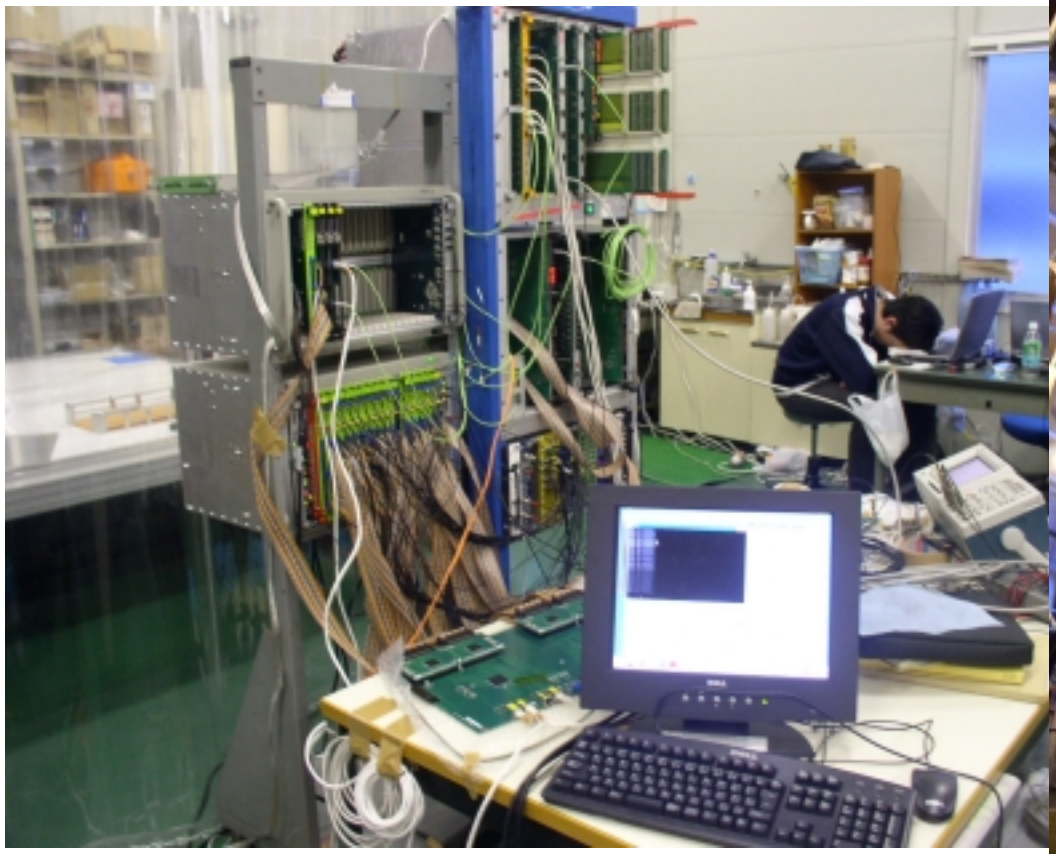


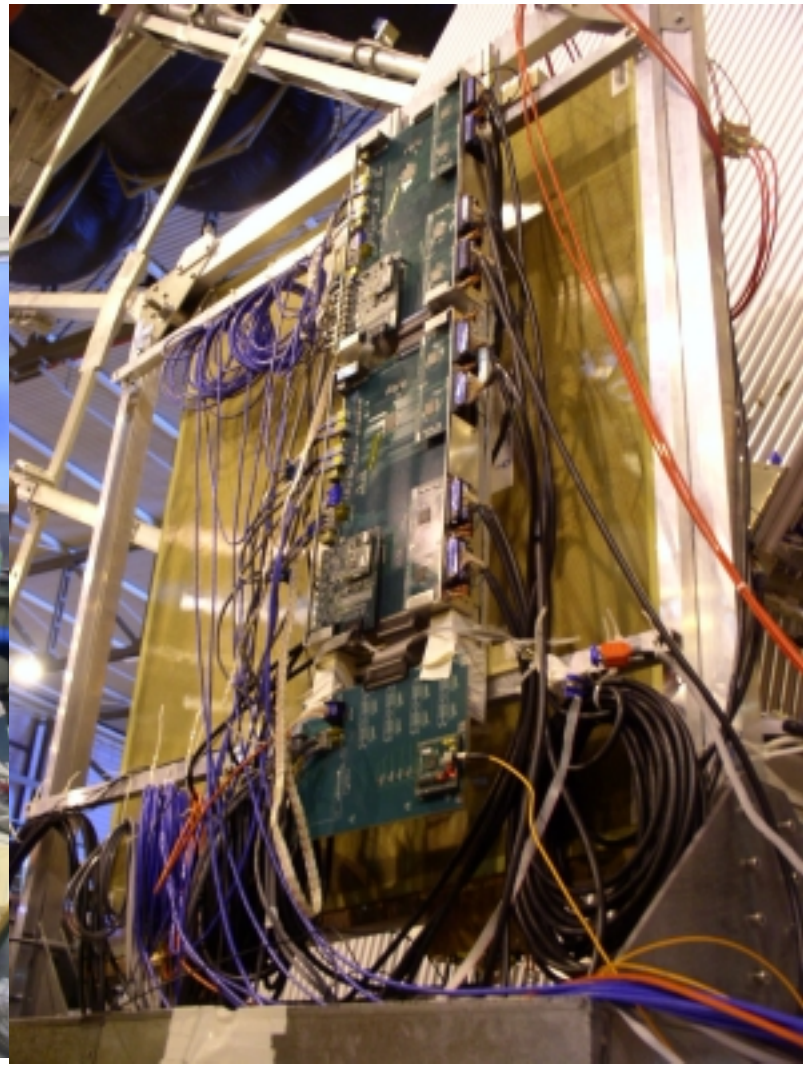
High density memory cell

4.5x4.5mm^2 core

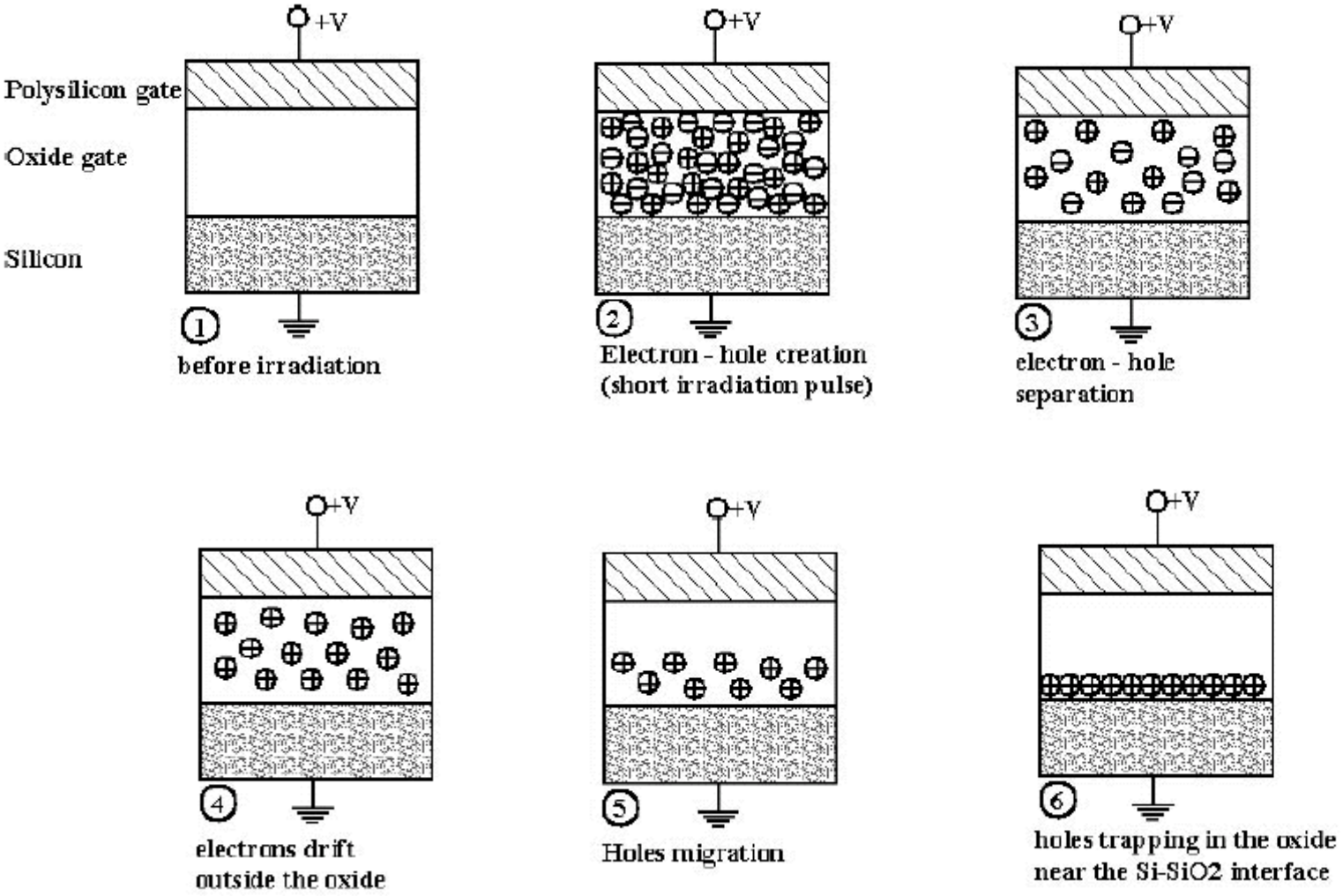


スライステスト・ビームテスト



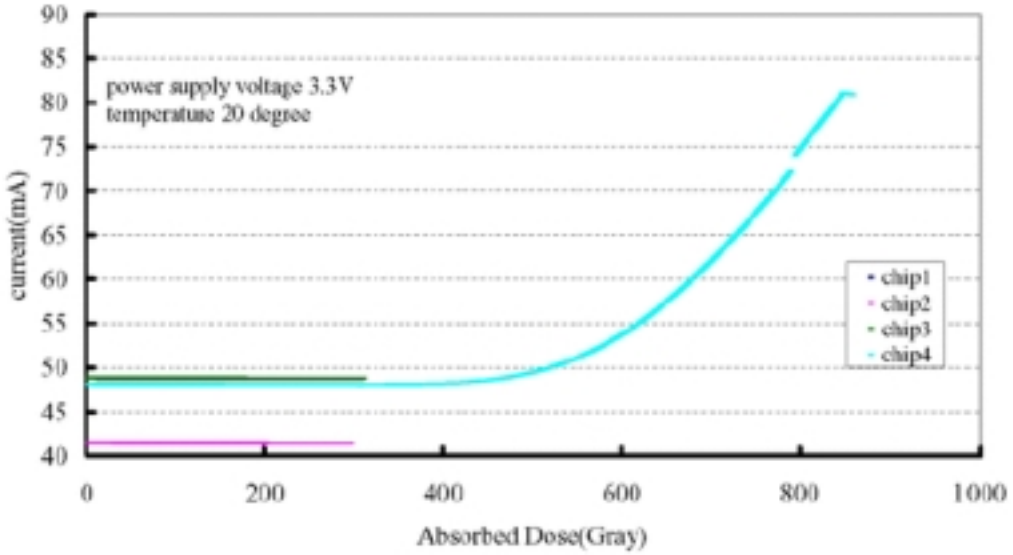


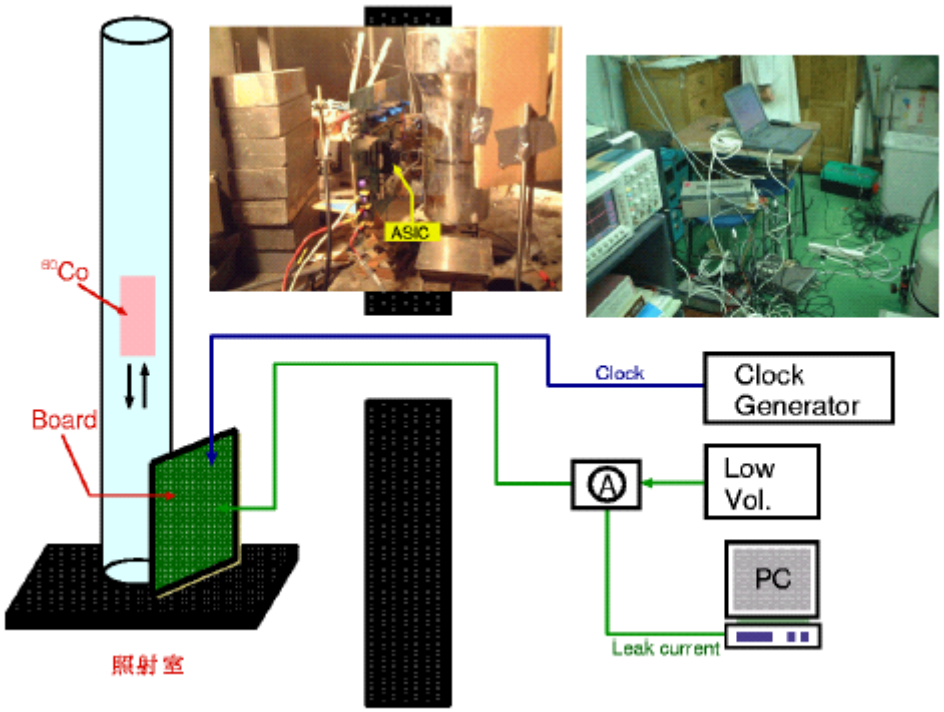
TID (Total Ionization Doze)

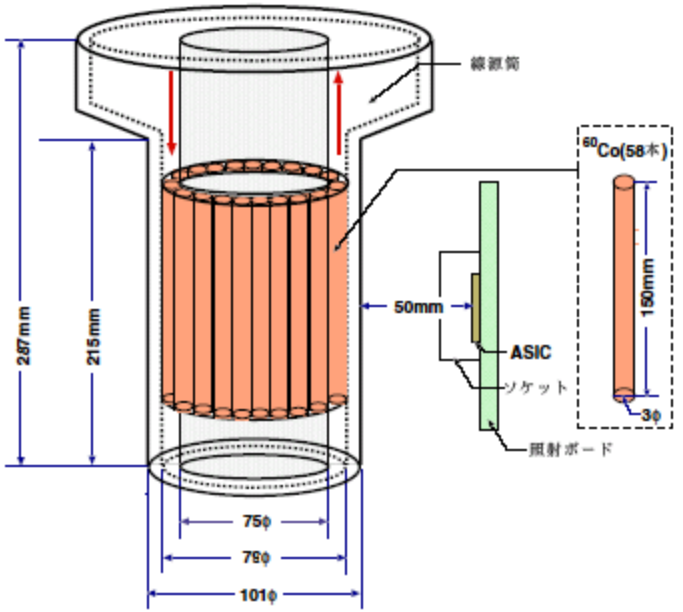


TIDスタディ

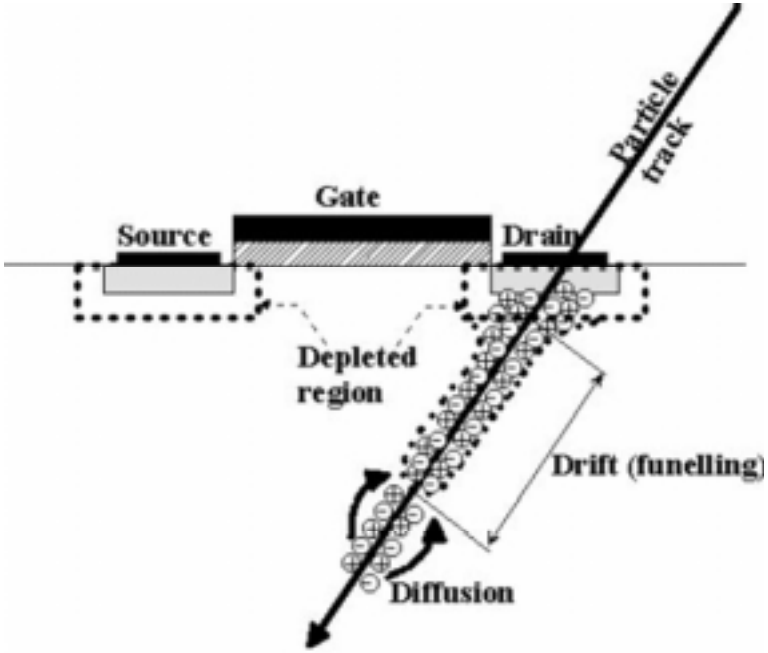
- 東大原子力総合センター
- Co60線源
- 22TBq







Single Event Effect (SEE)



Funelling in MOS :

Transient pulse **in a node**

=> upset in SRAM (latches)

and error in logic circuits.

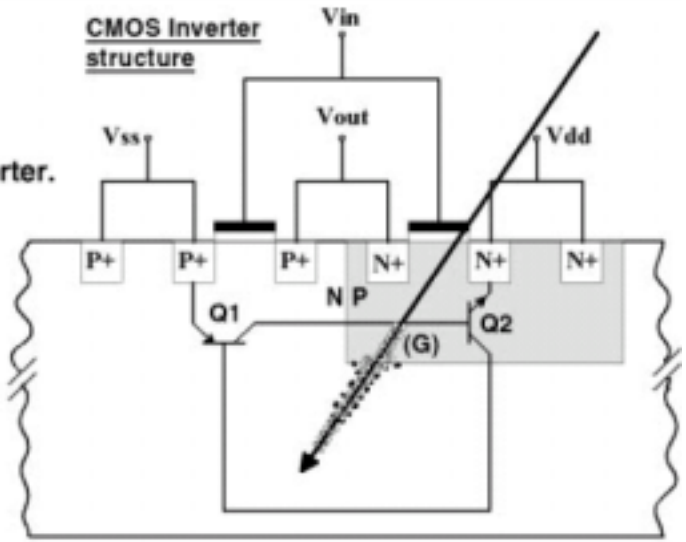
Single Event Upset (SEU)

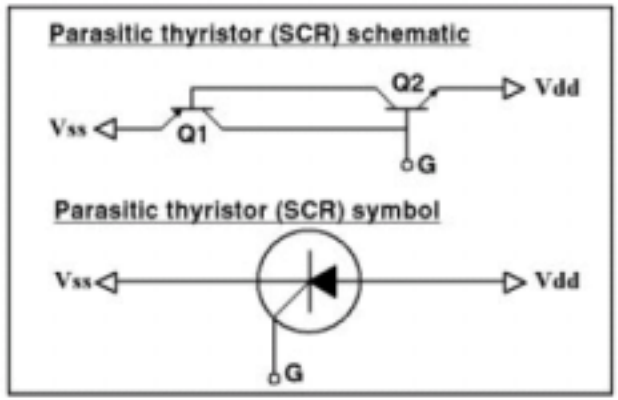
SEL: A highly ionizing particle trigger the parasitic thyristor contained in a bulk CMOS inverter.

=> Vdd-to-Vss short circuit.

Destructive mechanism if no current limitation.

Possible recovery by bias switch-off if the circuit is protected by a current limiter.

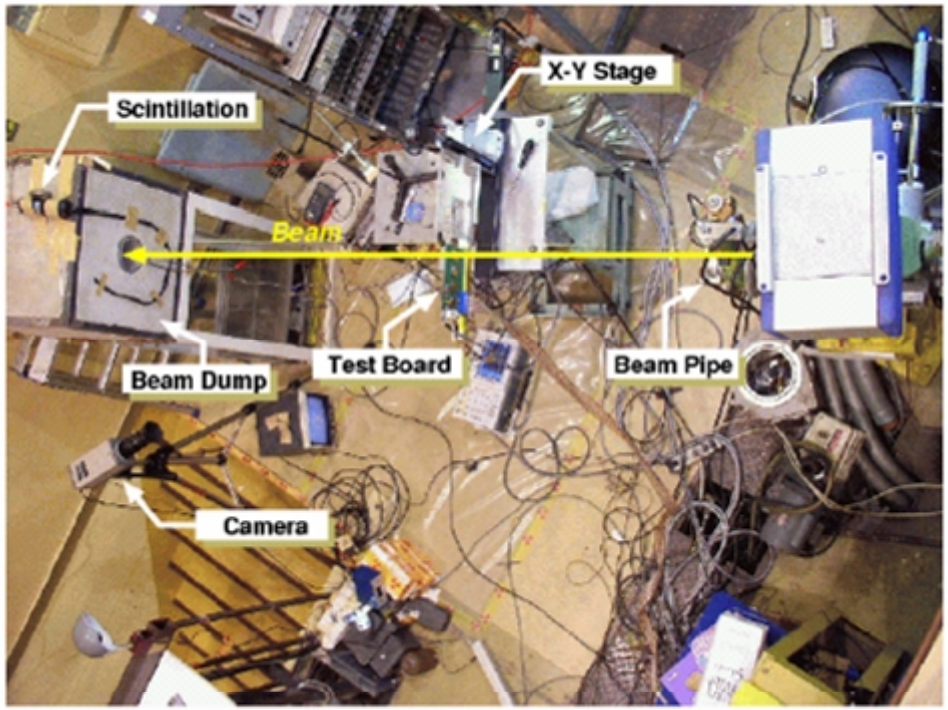




Single Event Latchup (SEL)

SEEスタディ

- 東北大サイクロ
- 70MeVプロトンビーム
- ～1nAビーム

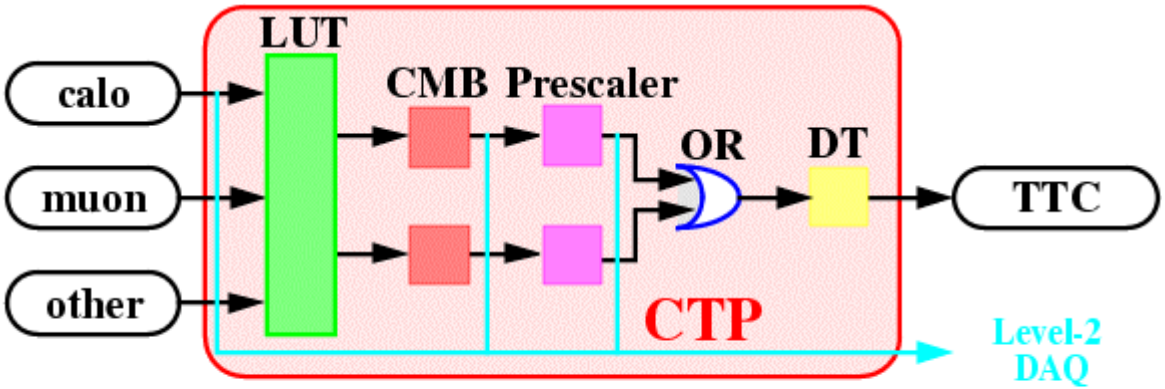


チップ名	フルエンス $[1/cm^2]$	ラッチアップの有無	レジスタの状態	レジスタ数	SEUの発生数	$\sigma_{SEU}[cm^2/bit]$
JRC(Chip1)	1.69×10^{12}	None	All-0	1024	79	4.6×10^{-14}
JRC(Chip2)	1.60×10^{12}	None	All-1	1024	18	1.1×10^{-14}
JRC(Chip3)	1.49×10^{12}	None	All-0	1024	69	4.5×10^{-14}
JRC(Chip4)	1.51×10^{12}	None	All-1	1024	19	1.2×10^{-14}
Total	6.29×10^{12}	None			185	2.8×10^{-14}

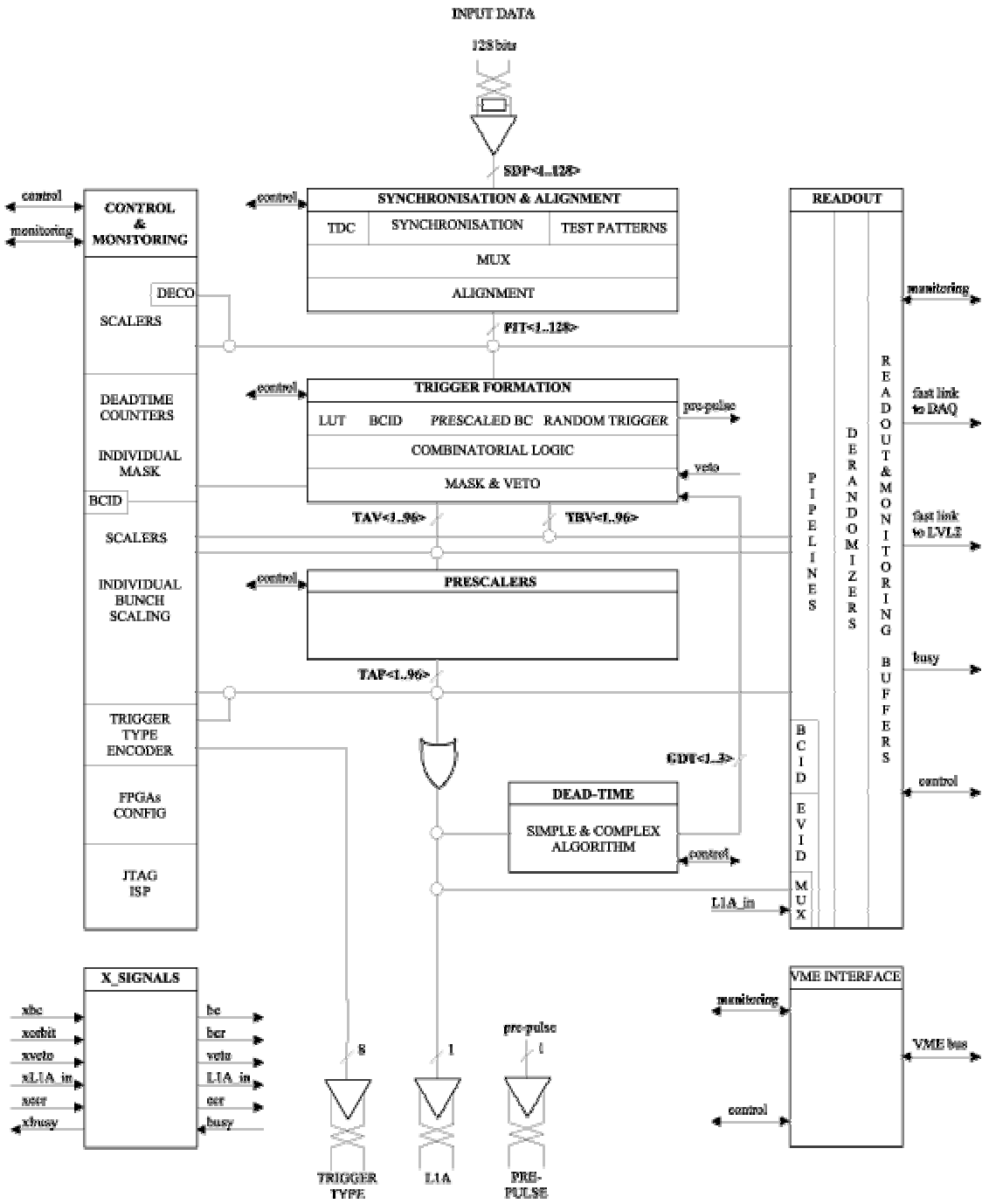
表 6.2.3: SEU 段面積の計算結果

セントラルトリガープロセッサ

- レベル1トリガーの最終判定機構
  - η-ϕ情報
  - ROIの決定
  - L1A(Level 1 Accept)の生成

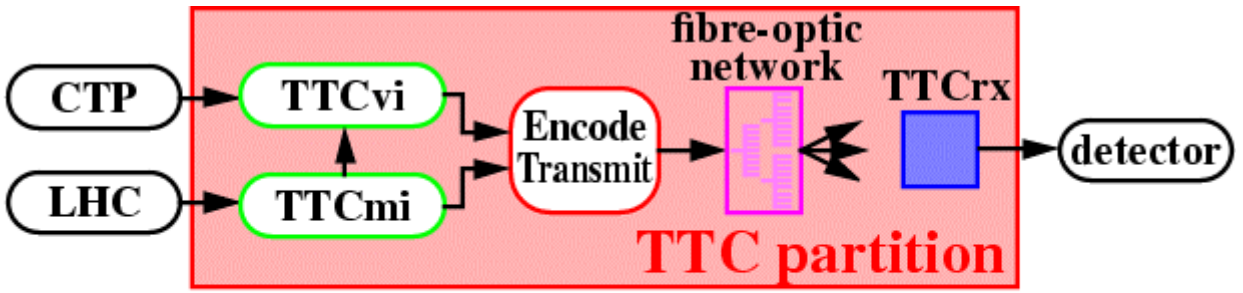


LUT Look-up Table
CMB Combinatorial Logic Device
DT Deadtime Logic

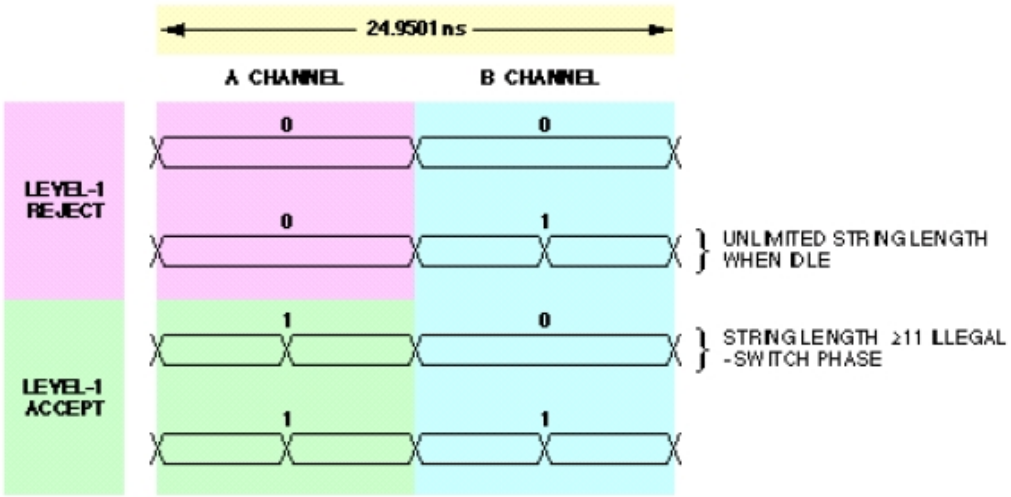

INPUT DATA
128 bits
SDP<1..128>
control
monitoring
CONTROL & MONITORING
DECO
SCALERS
DEADTIME COUNTERS
INDIVIDUAL MASK
BCID
SCALERS
INDIVIDUAL BUNCH SCALING
TRIGGER TYPE ENCODER
FPGAs CONFIG
JTAG ISP
SYNCHRONISATION & ALIGNMENT
TDC
SYNCHRONISATION
TEST PATTERNS
MUX
ALIGNMENT
FIT<1..128>
TRIGGER FORMATION
LUT
BCID
PRESCALED BC
RANDOM TRIGGER
COMBINATORIAL LOGIC
MASK & VETO
pre-pulse
veto
TAV<1..96>
TBV<1..96>
PRESCALERS
TAP<1..96>
GDT<1..3>
DEAD-TIME
SIMPLE & COMPLEX ALGORITHM
L1A_in
READOUT
PIPELINES
DERANDOMIZERS
READOUT&MONITORING BUFFERS
BCID
EVID
MUX
monitoring
fast link to DAQ
fast link to LVL2
busy
control
X_SIGNALS
xbc
xorbit
xveto
xL1A_in
xrst
xbusy
bc
bcr
veto
L1A_in
rst
busy
8
1
1
TRIGGER TYPE
L1A
PRE-PULSE
VME INTERFACE
monitoring
control
VME bus

トリガータイミングコントロール

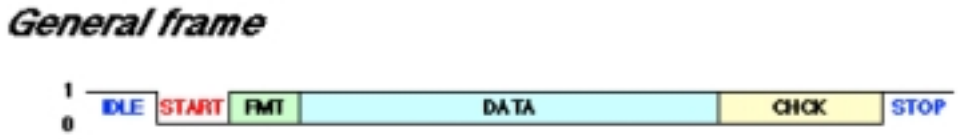
- TTC (Trigger Timing Control)
  - LHCクロックの供給
  - L1A (Level 1 Accept)信号の供給
  - BCR (Bunch Counter Reset)
  - ECR (Event Counter Reset)
  - Test Pulse

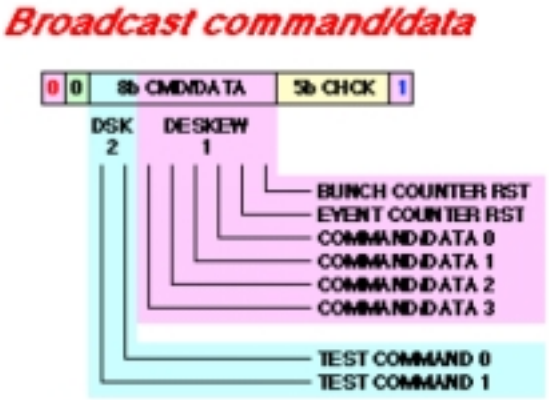


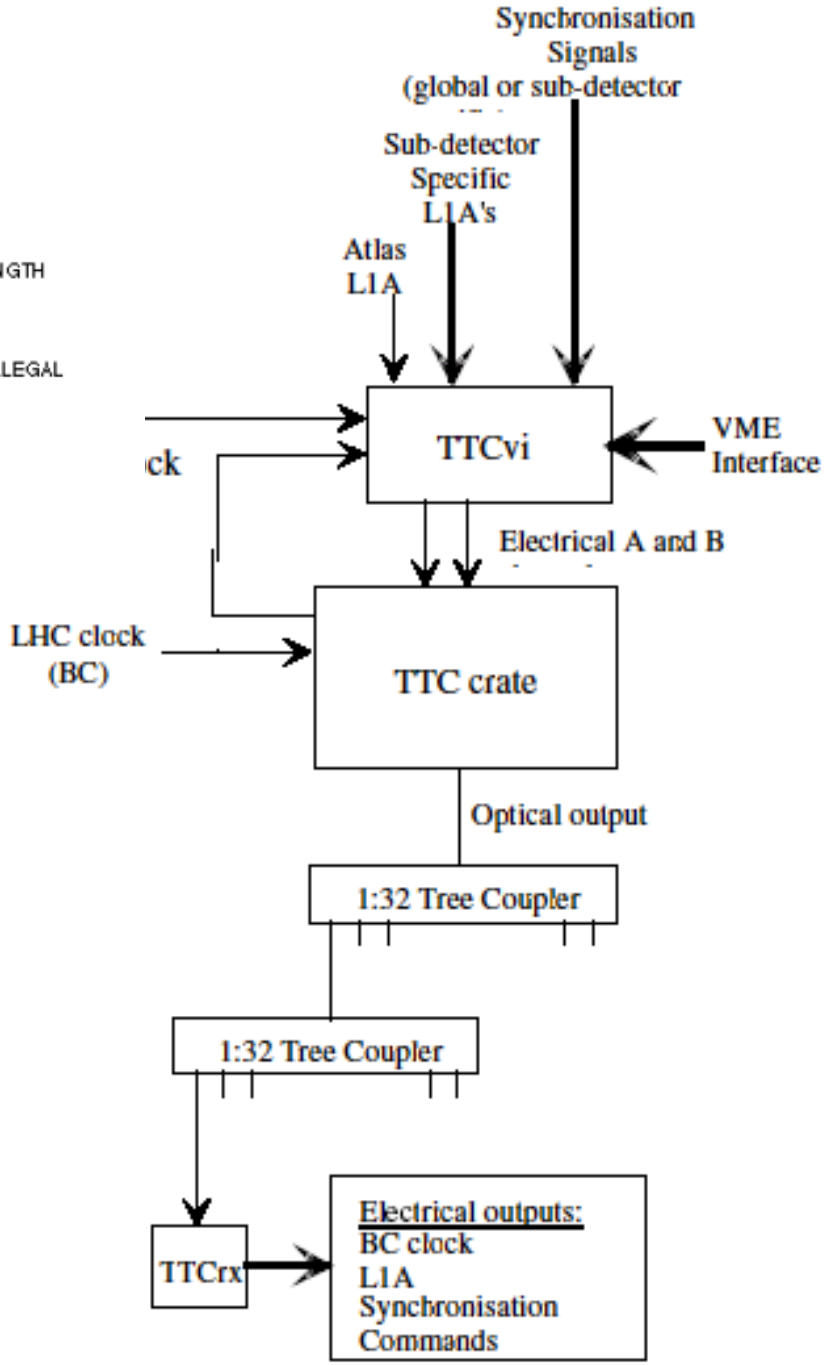
TTCvi VME Interface
TTCmi Machine Interface
TTCrx Receiver Chip



TTC Data Format



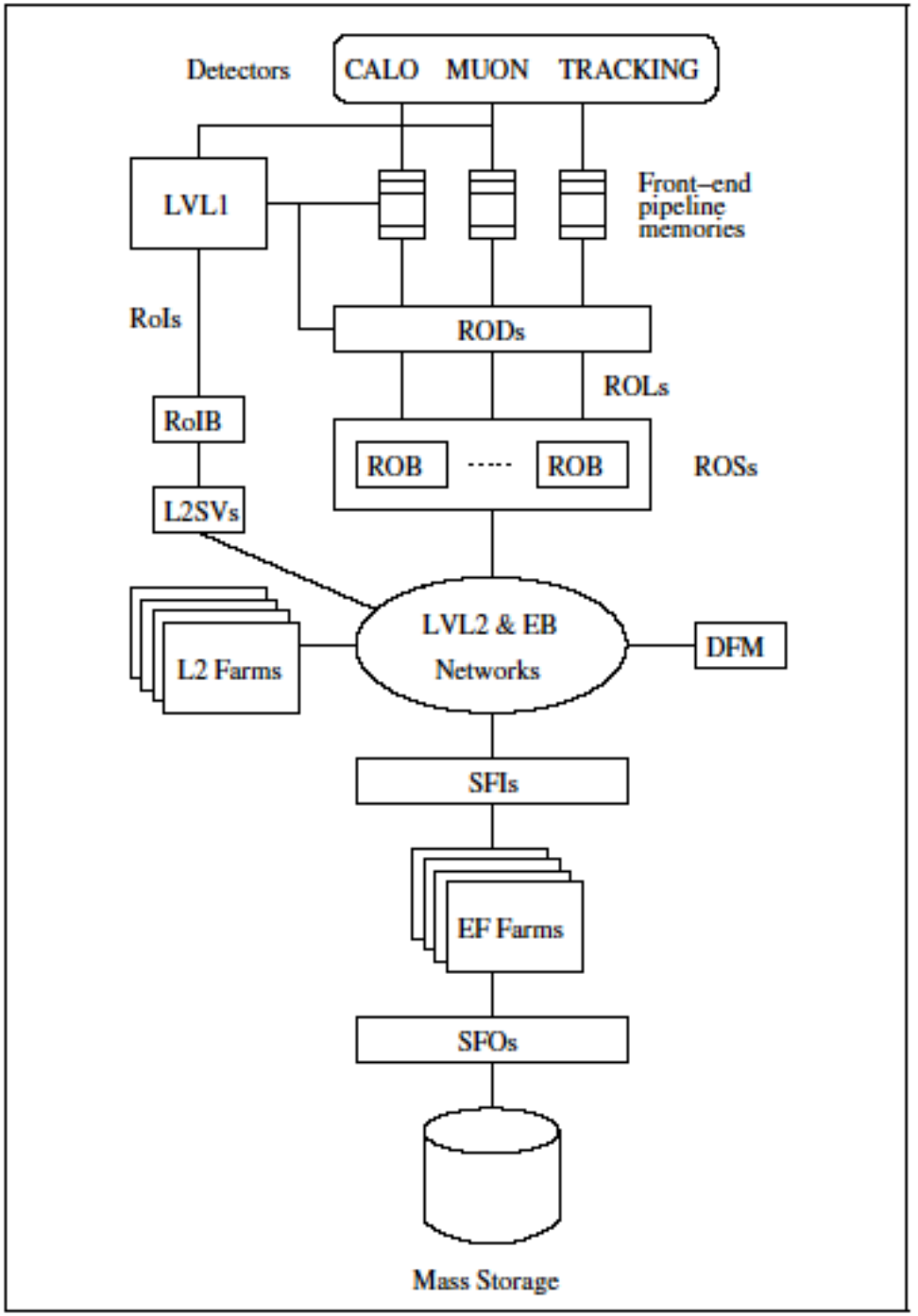




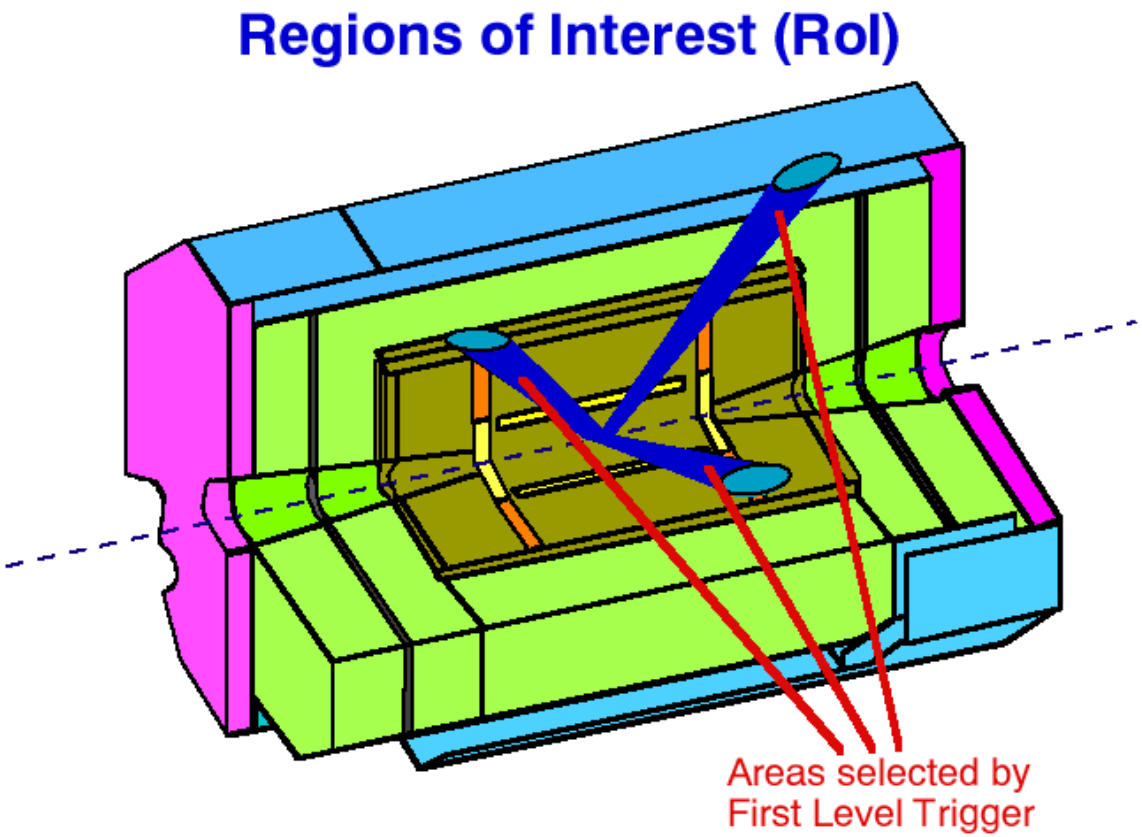
DAQ・高位トリガー

- ROD: Read Out Driver
- ROL: Read Out Link
- ROB: Read Out Buffer
- ROS: Read Out System
- RoI: Region of Interrest
- RoIB: RoI Builder
- L2SV: Level 2 Superviser
- DFM: Data Flow Manager
- SFI: SubFarm Interface
- EF: Event Filter
- SFO: SubFarm Output

詳細は長坂さんの話で



レベル2トリガーの戦略



まとめにかえて

- ATLAS実験トリガーシステム
  - バーティカルスライステスト
  - ビームテスト2003～2004
  - PRR (Production Readiness Review)
  - 量産2004年度
  - 組み込み2005年度～2006年度
- 資料
  - レベル1TDR
    - http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html
  - 高位トリガー・DAQ・検出器制御
    - http://atlas-proj-hltdaqdcs-tdr.web.cern.ch/atlas-proj-hltdaqdcs-tdr/