

PMC/PC を搭載した DAQ プラットフォーム

(The Data Acquisition Platform equipped PMC/PC)

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COLLABORATION

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Belle DAQ group

KEK Neutrino DAQ group

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University of Hawaii

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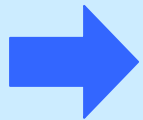
KRAKOW Institute of Nuclear Physics

Densan Co. Ltd.

Designtech Co. Ltd

Motivation

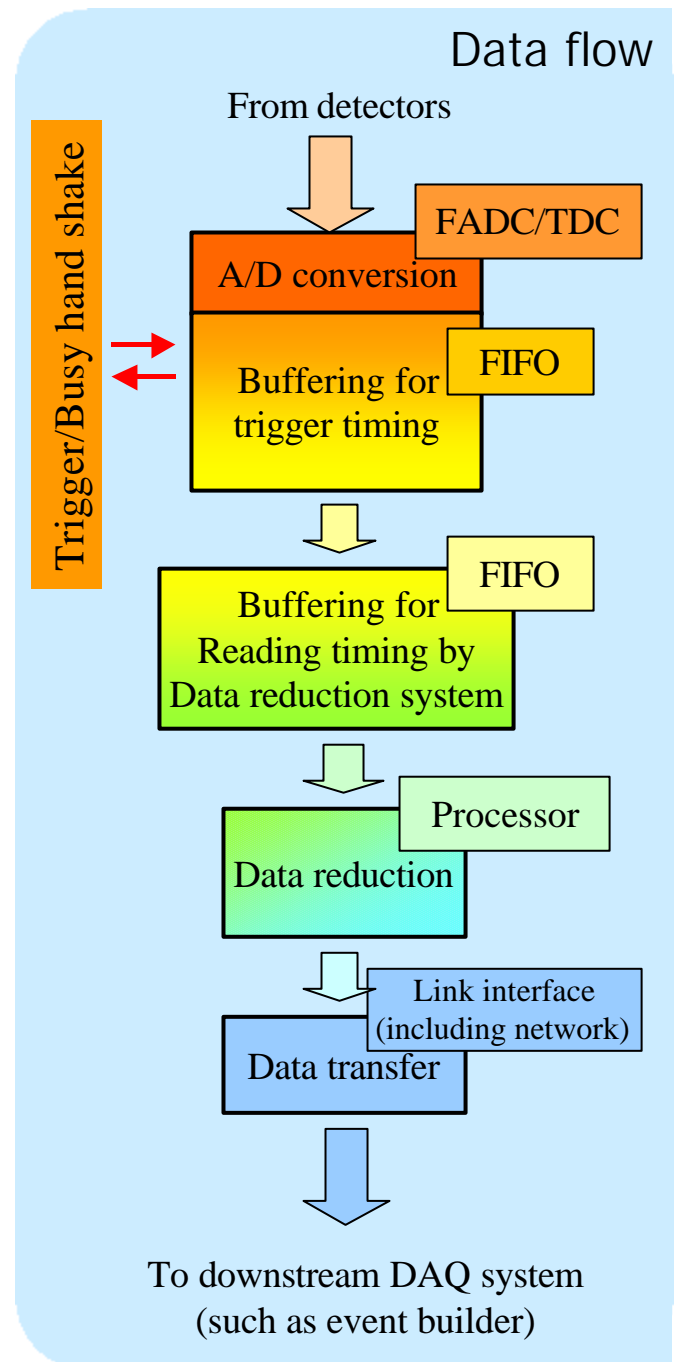
- DAQ scale of the next-generation physics experiments in KEK
 - Experiments of J-PARC (JHF/50Gev PS)
 - 500Hz ~ 10kHz trigger, 1k ~ 10k channel
 - Super KEKB (luminosity $\sim 10^{35}\text{cm}^{-2}\text{s}^{-1}$)
 - $\sim 10\text{kHz}$ trigger, $\sim 100\text{k}$ channel
- Traditional specifications does not fit.
 - Cost
 - Maintenance
 - Standard
 - Channel density



We started to develop a widely usable DAQ system.

Concept

- Working under 10kHz trigger
 - Front-end Buffering
 - Waiting trigger decision
 - Buffering trigger non-uniform timing
 - Buffering behind non real-time system
 - On-board data reduction
- Wide scalability
 - From small test experiments to large experiments such as Super KEKB experiment
- Modular system
 - Maintenance, upgrading
- Using standard and commercially available technologies
 - Easy to follow evolution of technology
 - Cost effectiveness
 - Production, maintenance, upgrading
- High channel density : ~100 ch/board



Form Factor and Power Supply

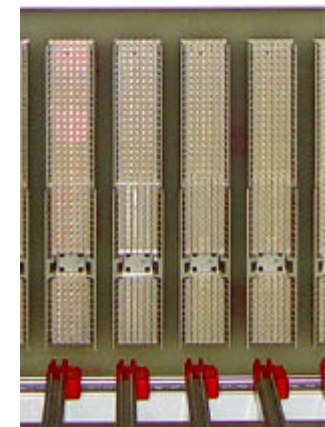
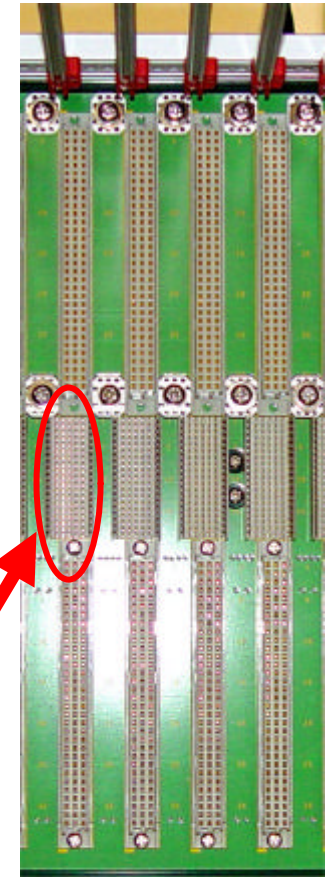
- 9U Euro card/crate
 - Cost effectiveness
 - There are 6U type.
 - VME-32 bus
- J0 Connector for Power Supply
 - To treat front-end analog-digital conversion devices



Voltage	-5.0V	-3.3V	+3.3V
Total Max Current	100A	320A	200A

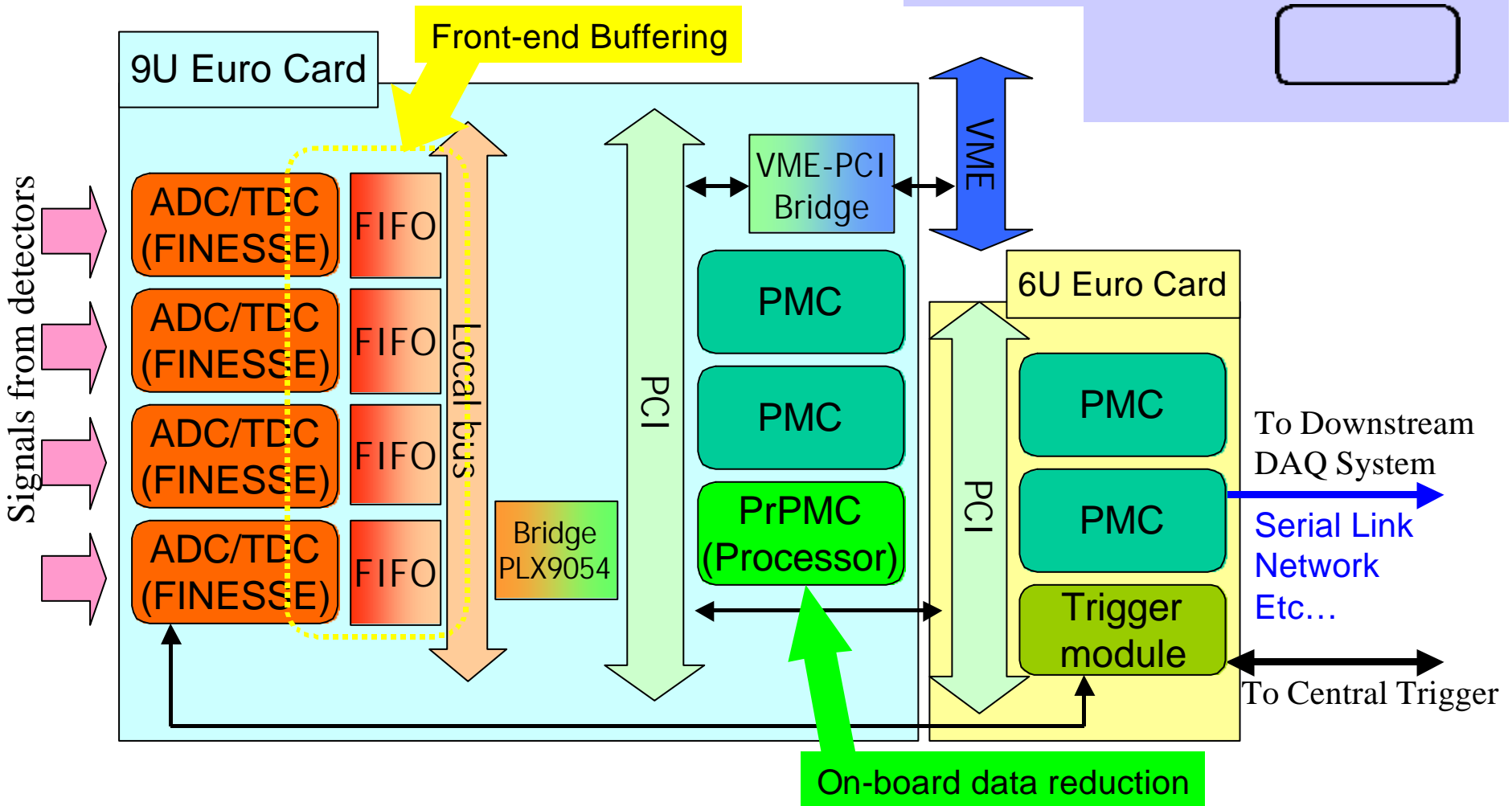
Pos.	z	a	b	c	d	e	f
1	GND	GND	GND	GND	GND	GND	GND
2	GND	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND
4	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
5	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
6	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
7	GND	+3.3V	+3.3V	GND	GND	GND	GND
8	GND	GND	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	-3.3V	-3.3V	GND
11	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
12	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
13	GND	GND	GND	GND	GND	GND	GND
14	GND	-5V	-5V	-5V	-5V	-5V	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	S1+	S1-	GND	S2+	S2-	GND
17	GND	S3+	S3-	GND	S4+	S4-	GND
18	GND	S5+	S5-	GND	S6+	S6-	GND
19	GND	S7+	S7-	GND	S8+	S8-	GND

Pin assignment of power supply connector (IEC 61076-4-101)



Prototype Read-out module schematic

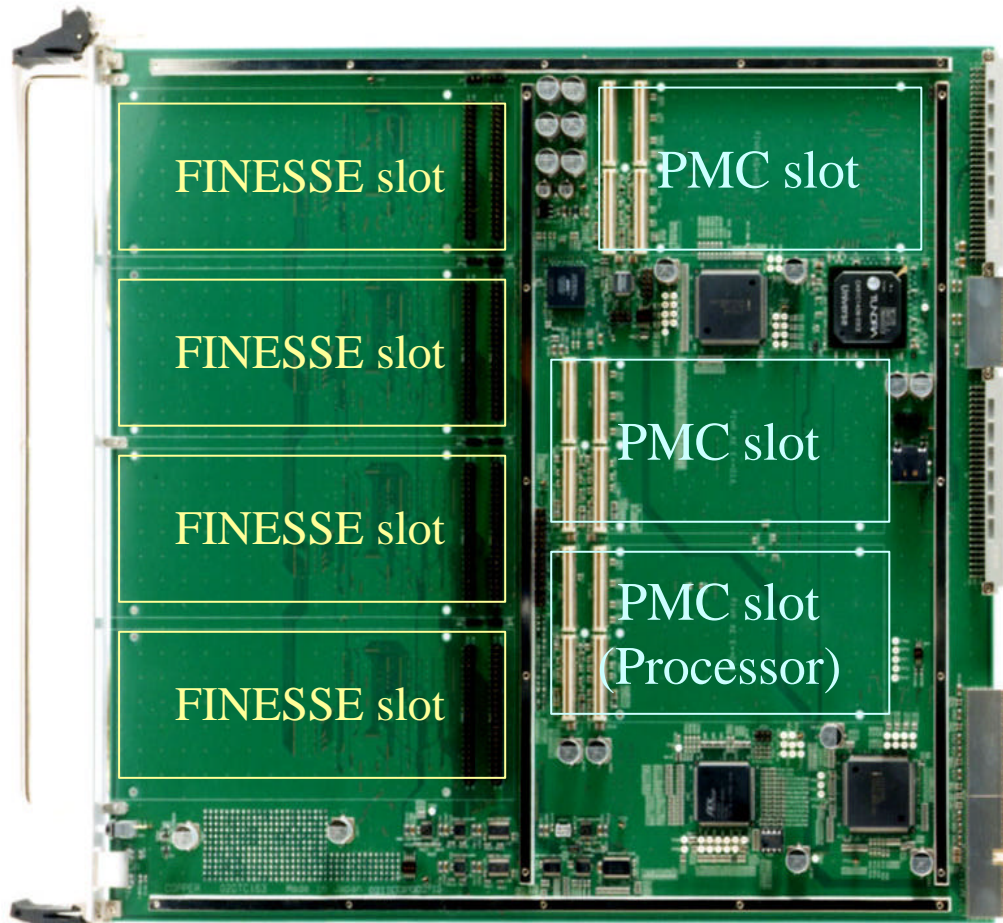
- Standard components
 - 9U Euro card
 - VME-32 compatible
 - PCI
- Module structure



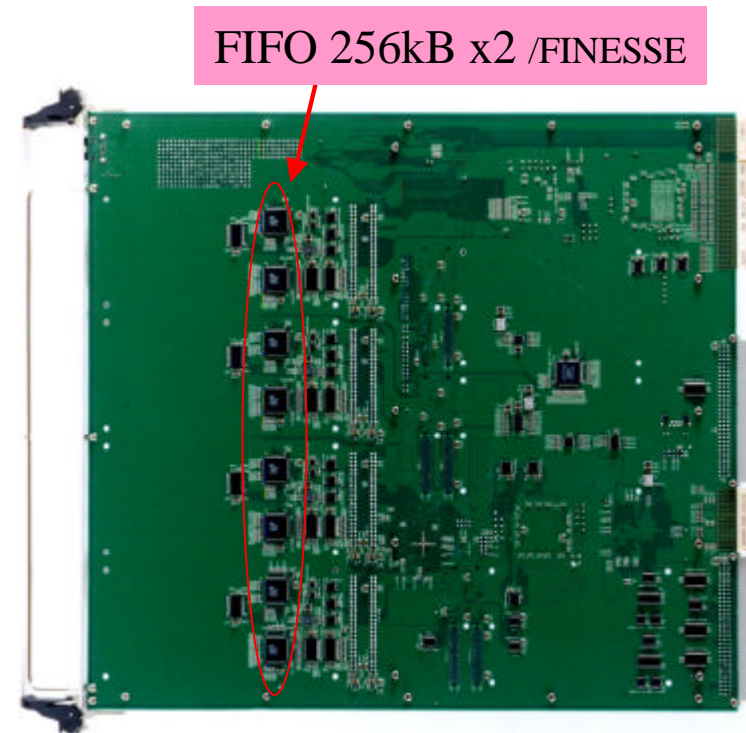
COPPER

Main Mother Board of Read-out Module

- 4 Front-end AD card slot
- 2 general PMC slot
- 1 Processor PMC slot
- VME interface
- 512kB x 4 FIFO
- 32bit 33MHz PCI



UP SIDE

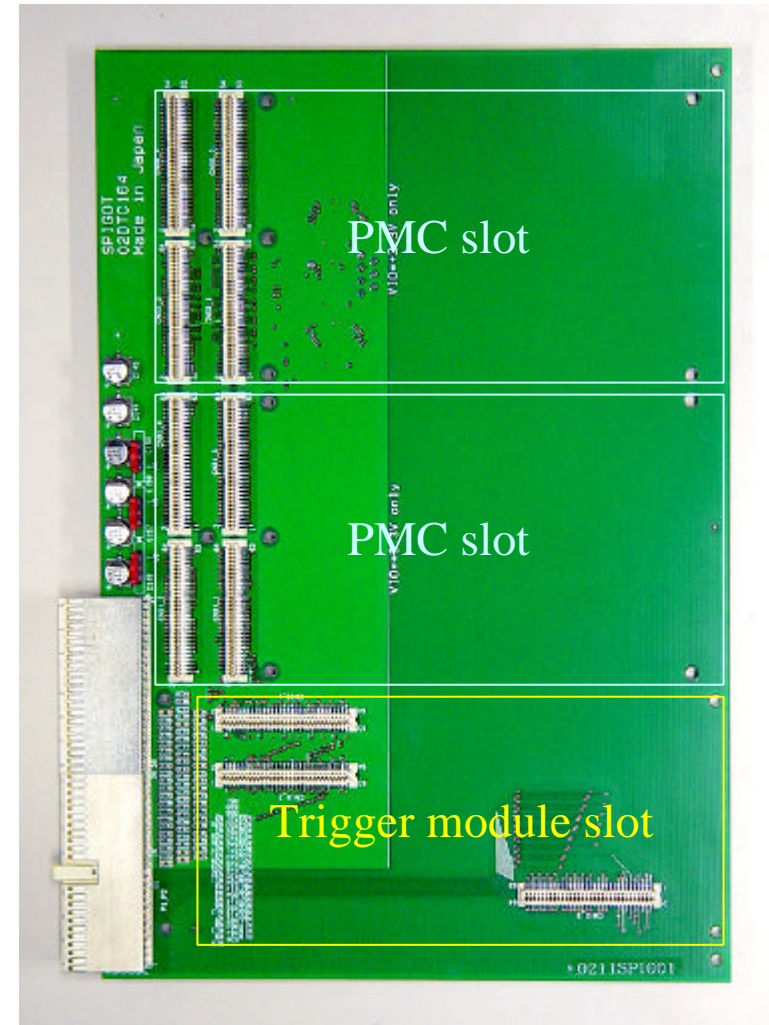
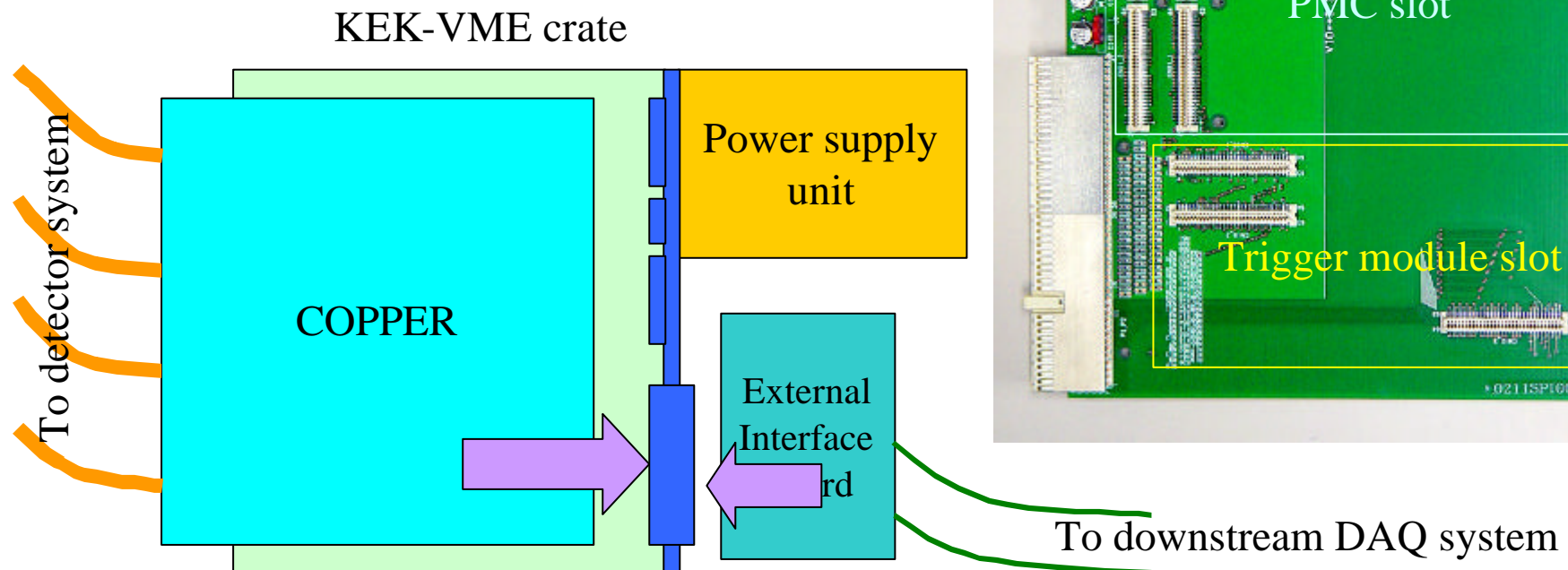


DOWN SIDE

External Interface board

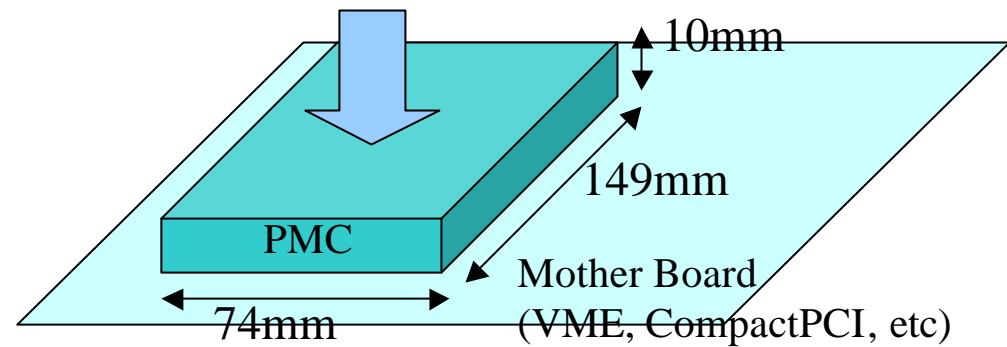
Rear side Mother Board of Read-out Module

- 2 PMC slot
 - Data transfer interface
 - 100Base/Gigabit Ethernet
 - Serial link (IEEE1394 etc)
- 1 Trigger module slot

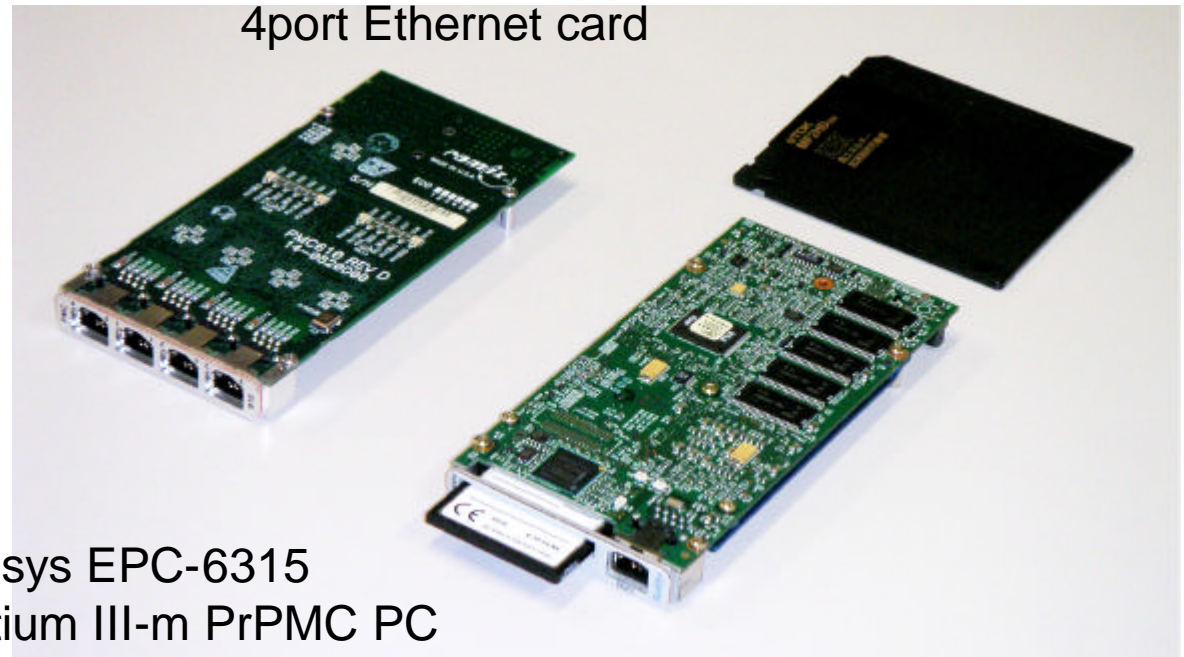


PMC

- PCI Mezzanine Card, IEEE1386.1
 - PCI compliant
 - Several modules are commercially available with reasonable price
 - Processor (PPC/x86/...)
 - 100Base/Gigabit Ethernet
 - IEEE1394
 - Etc....



Ramix PMC610
4port Ethernet card



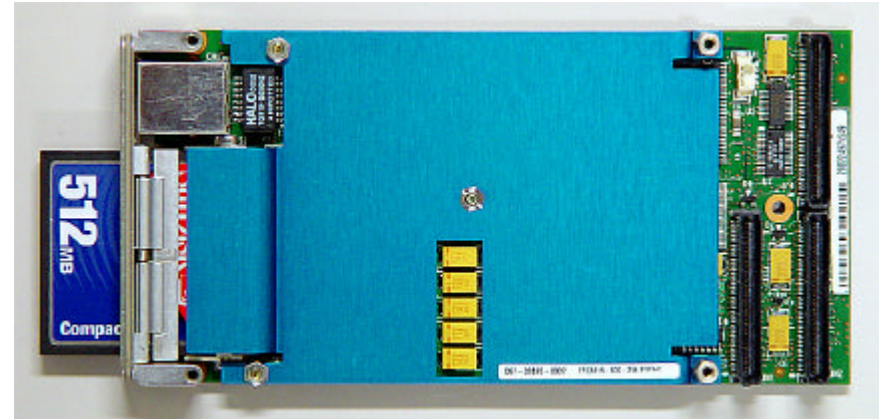
Radisys EPC-6315
Pentium III-m PrPMC PC

Processor PMC

PC architecture

- It is familiar for many person.
 - same architecture as the commodity PC.
- Rich functional OS runs on PC.
 - Linux, vxworks, etc...
 - We can develop applications easily and drive many complex devices (such as Ethernet TCP/IP).
- PC is the main stream of the commerce.
 - It is easy to get faster processors at a low price.
- Lots of know-hows openly available.

We use **Linux 2.4** on Radisys EPC-6315, which is processor PMC card, for on-board data reduction.



Radisys EPC-6315

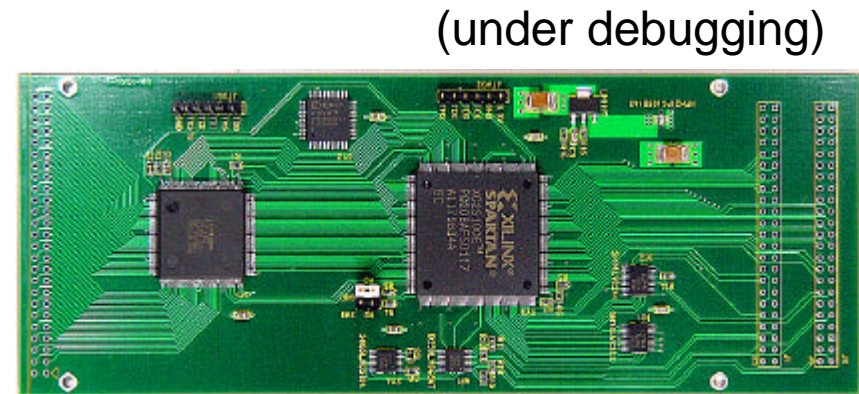
- **800 MHz Pentium IIIm Processor.**
- 512 kB secondary (L2) cache.
- 133 MHz FSB and Memory Bus.
- Up to 512 MB SDRAM with ECC.
- 10/100 BaseT Ethernet port
- On-board Compact Flash socket.
- Dual USB 1.1 ports.
- Integrated watch dog timer and real time clock.
- 32-bit 33/66 MHz PCI bus interface.

FINESSE

Front-end daughter card

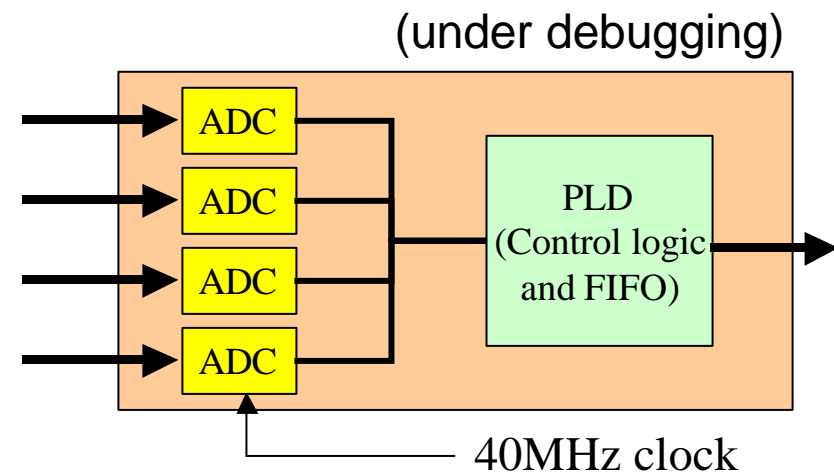
- Time Memory Cell (TMC) based pipeline TDC

- TMC : AMT2 (the latest TMC chip which is developed for ATLAS muon chamber)
- Input : 24ch LVDS
 - 96 ch/board
- Resolution: 0.78 ns/bit (at using 40 MHz clock)
- Trigger buffer depth: 8 words



- A prototype of flash ADC card.

- ADC: Analog Devices AD9235-20
- Resolution: 12bit
- Number of channel: 8
 - 32 ch/board
- Max sampling clock: 40MHz



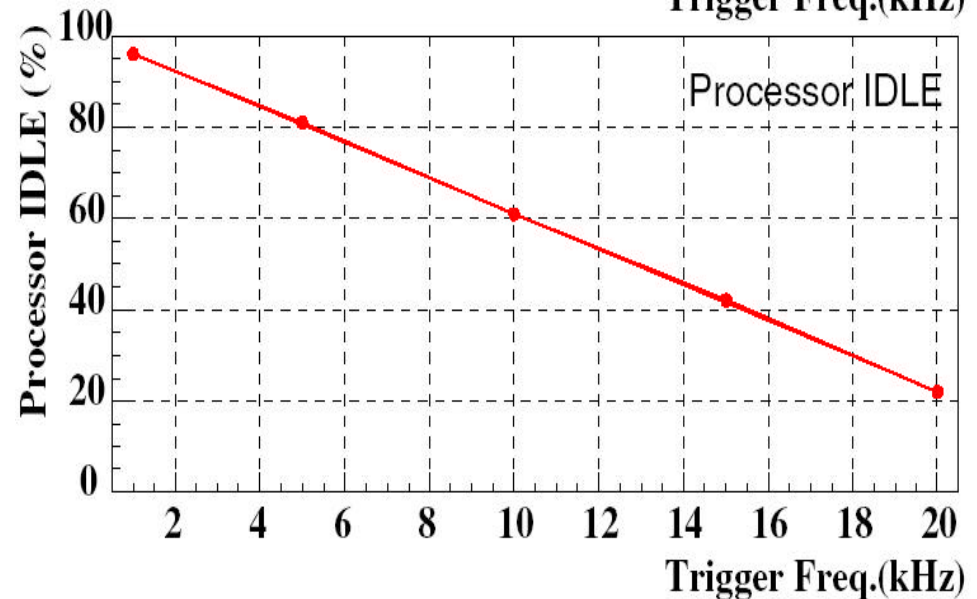
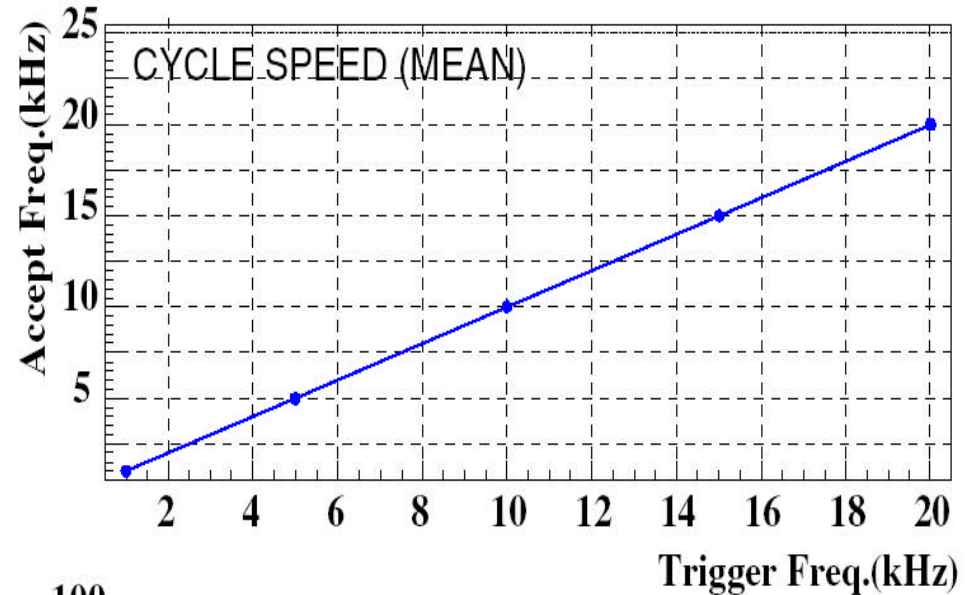
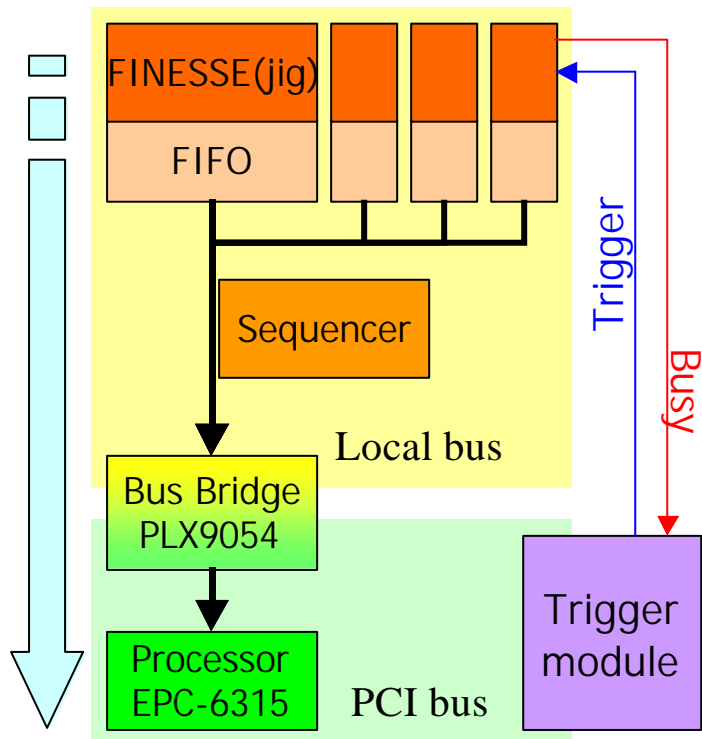
FINESSE

(under planning)

- 500MHz FADC
 - 8bit
 - 2ch/FINESSE
- Charge sensitive ADC
 - Current integrator type
- Analog memory cell
 - 1GHz sample
- 16bit wave form sampler
 - 5MHz sample
- High resolution TDC
 - 50psec
- DSSD pipeline front-end (CMS)

Performance Test

- Data size of this test
 - $208B * 4 = 832B$
- Basic speed of data transfer during DMA cycle
 - $\sim 80MB/sec$
- Working stably



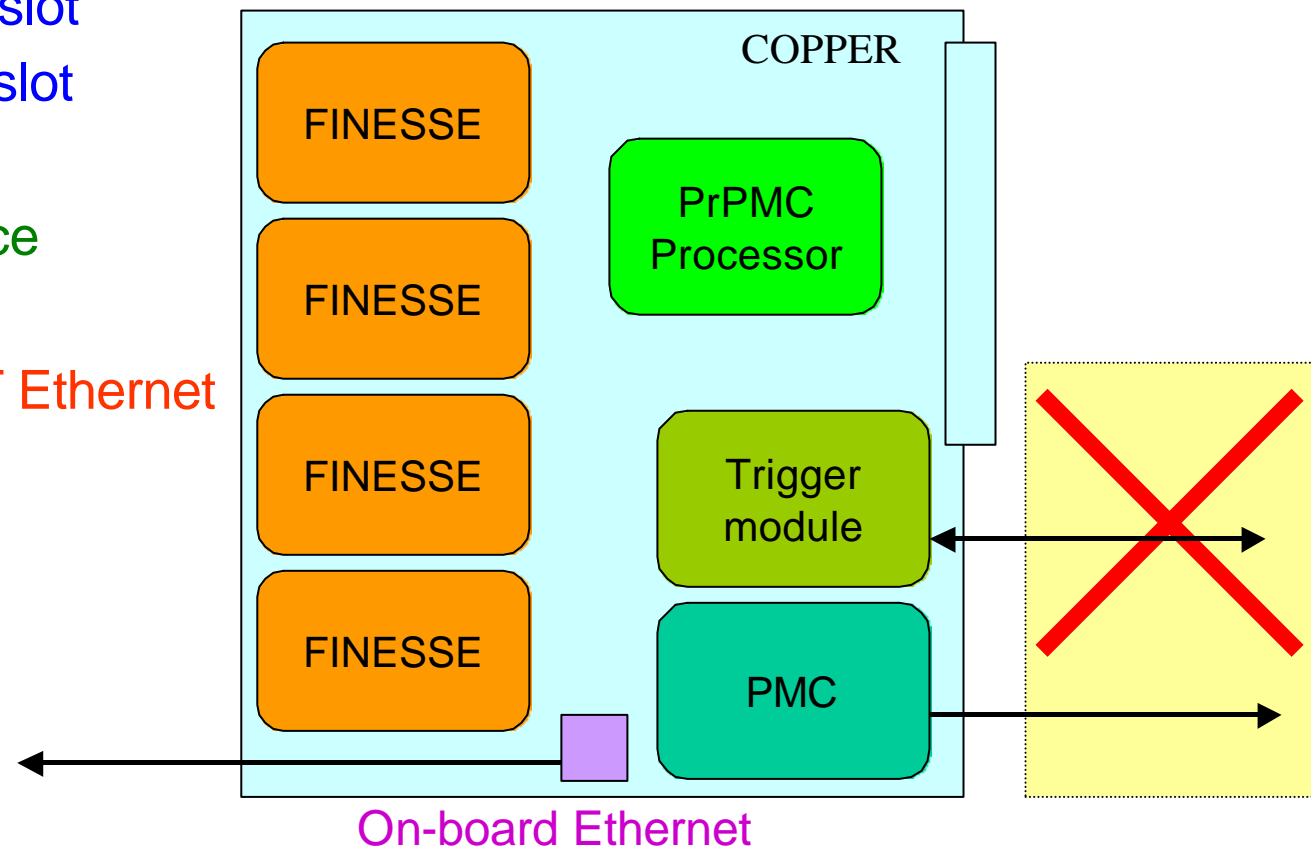
Summary

- We have developed a universal DAQ platform, which has PMC bus as the internal bus. The characteristics are:
 - Front-end buffering
 - PC architecture as on-board data reduction
 - Processor and data transfer interface that are upgradeable by adopting a modular structure
 - Flexibility and scalability that can be applied to a wide range of experiments
- The performance of data transfer from FIFO to processor main memory is **80MB/sec** without errors.
- This prototype system was tested up to **20kHz** trigger and **832B** event size using Pentium IIIm 800MHz
- We are developing a refined version of the system, practical front-end daughter cards, and trigger handling/distribution system.

Modification to Next version

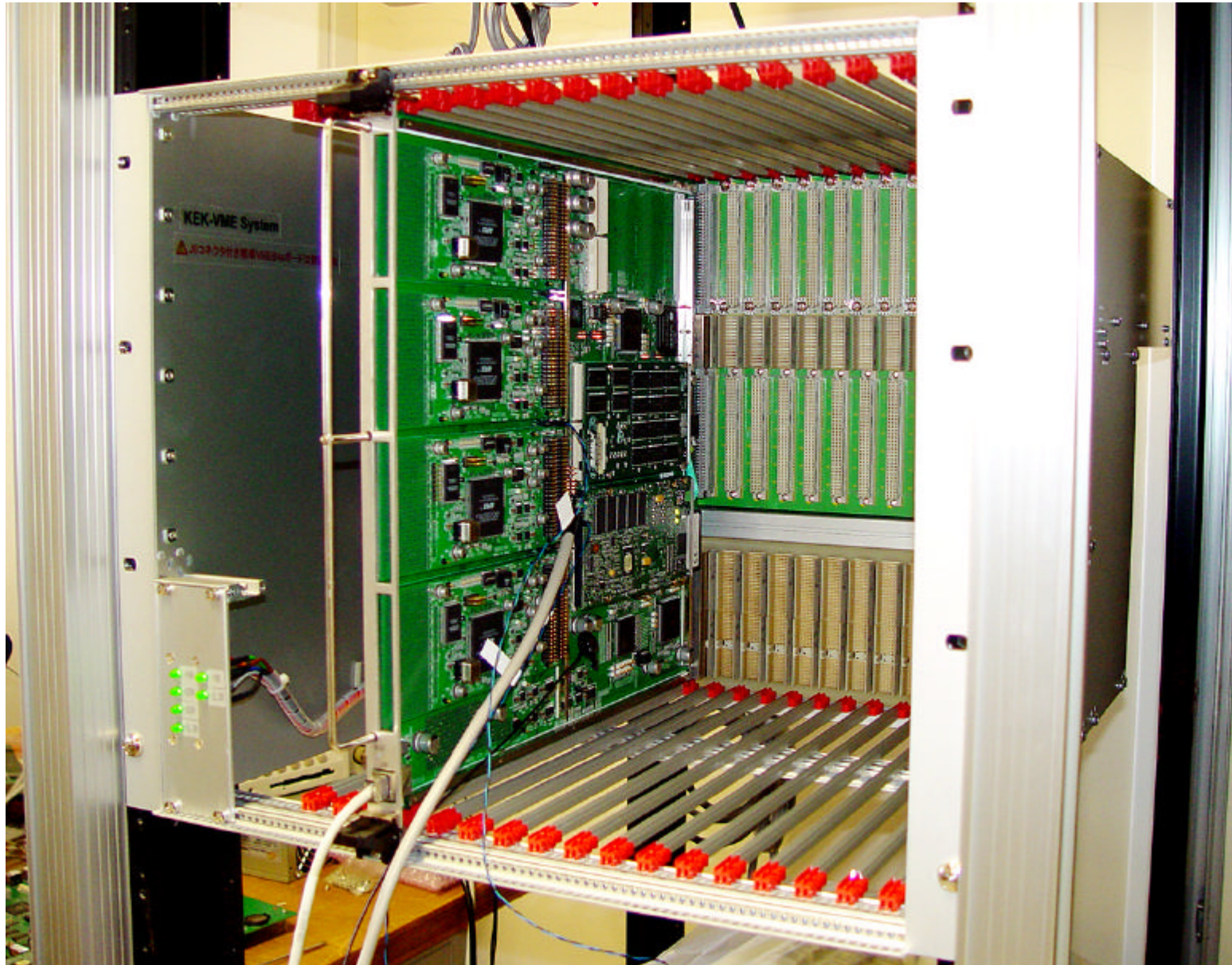
- COPPER and external interface board will be merged into next version COPPER

- One Trigger module slot
- One One Processor slot
- One general slot
 - data link interface
 - etc ...
- On-board 100base-T Ethernet



KEK-VME crate and Read-out modules

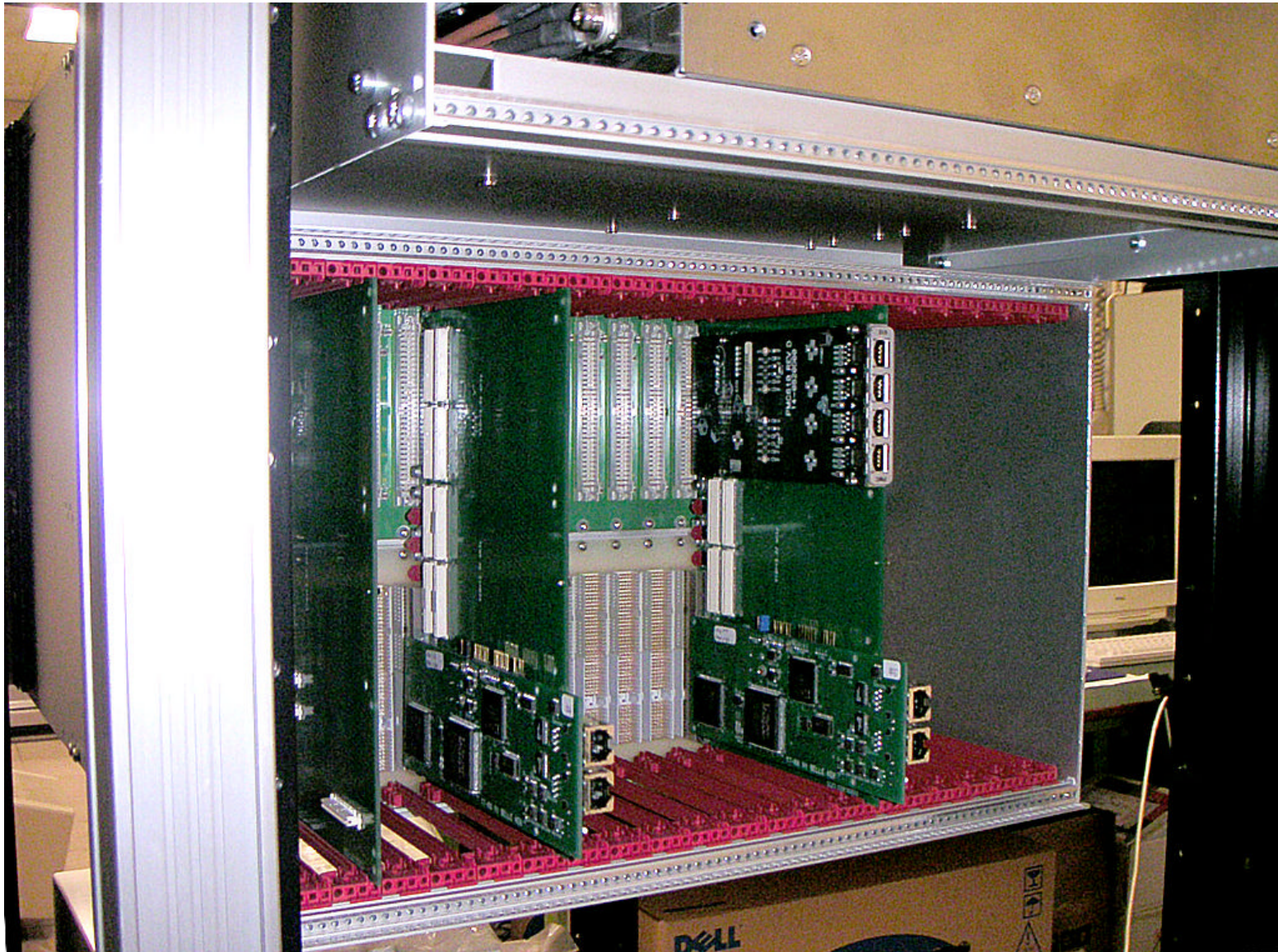
COPPER/FINESSE(jig)/EPC-6315/PMC-memory



Appendix

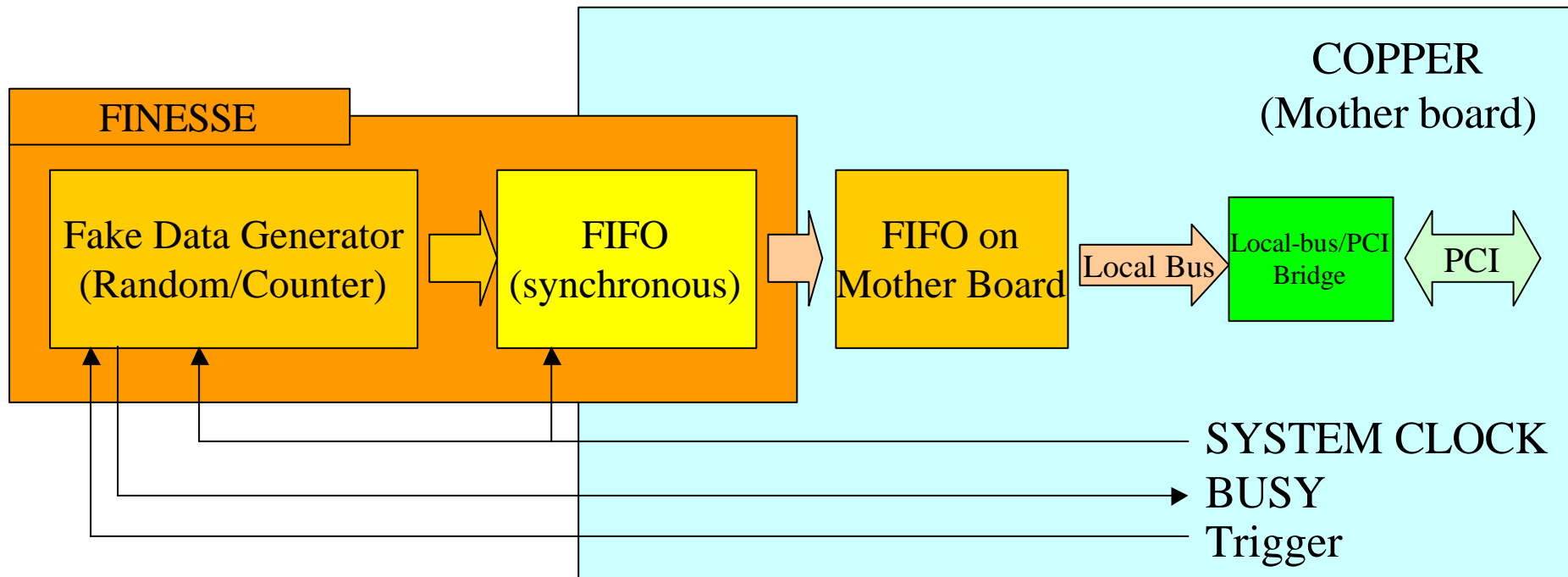
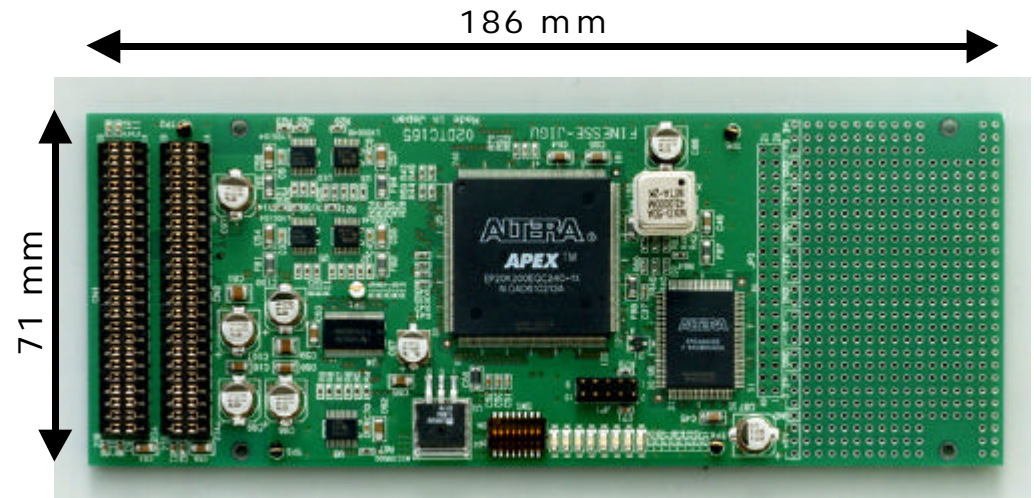
Back side of KEK-VME crate

SPIGOT/Trigger module/PMC 4-port LAN card



FINESSE(jig)

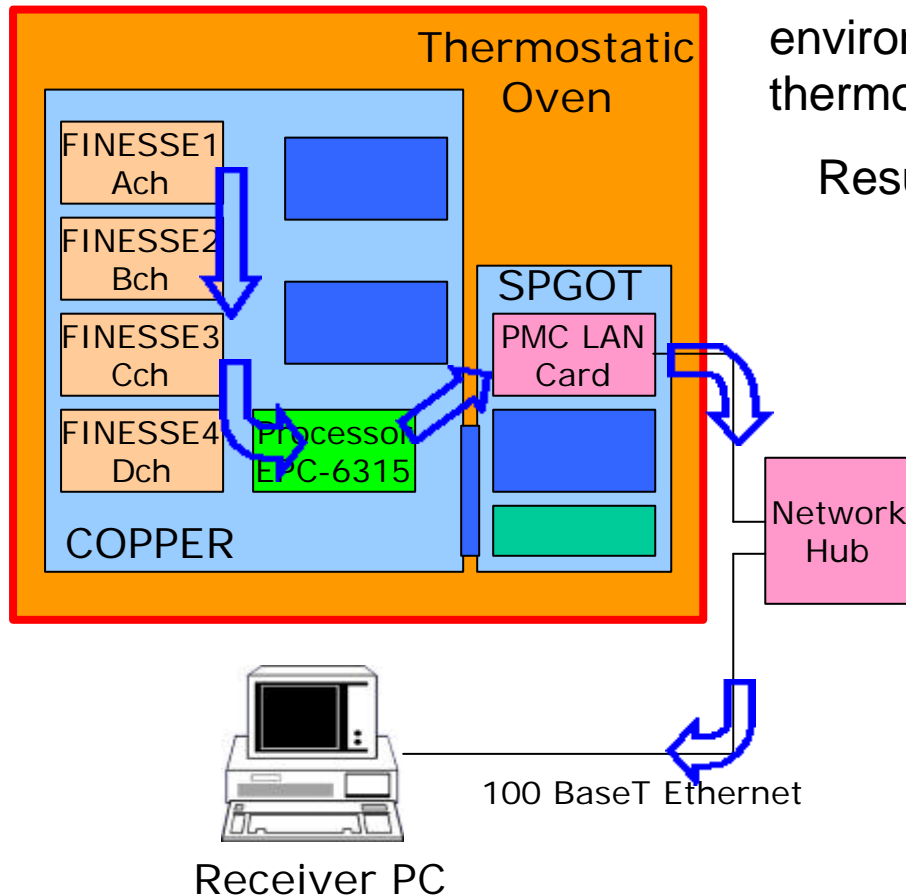
- Front-end daughter card for testing DAQ system
 - Making fake data
 - Trigger/busy hand-shake



Reliability Test

We tested reliability of the read-out modules. One is a 77 hour long run test, the other is a thermal test, with 10 Hz trigger. Data are read from FINESSE FIFO and sent to another computer via 100 BaseT network. Data go through FINESSE - Processor - LAN card on SPGOT - network - another PC. Thermal environment for the modules was changed by thermostatic oven according to a following graph.

Thermal Test Setup



Results are:

- 77 hour long run test : No Error
- Thermal test : No Error .

